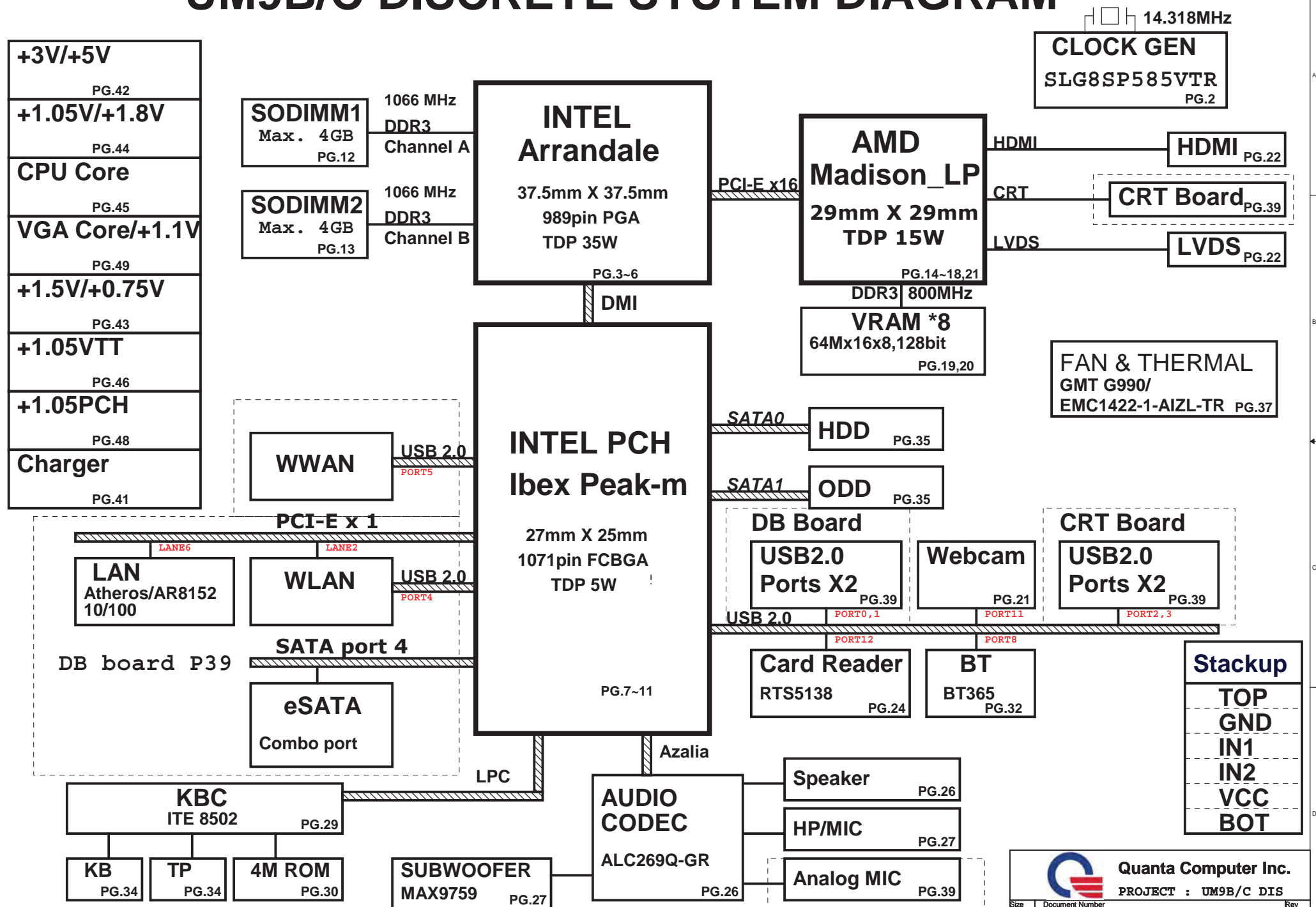
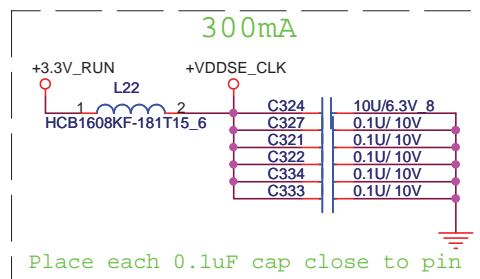
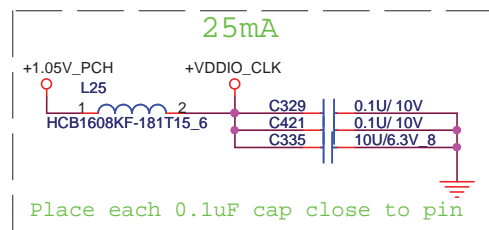
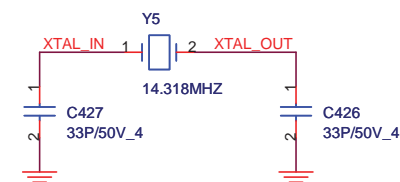
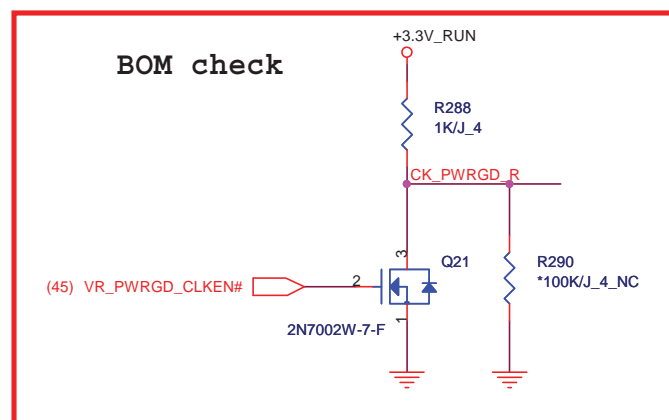
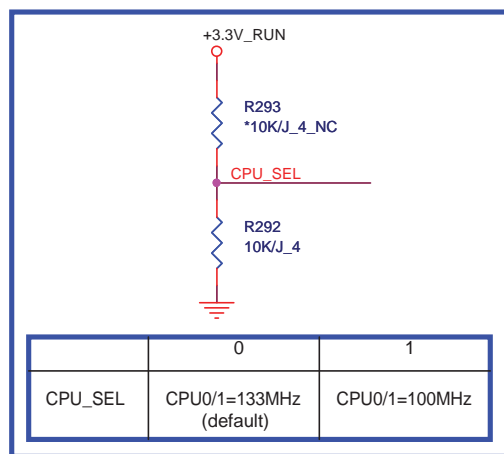
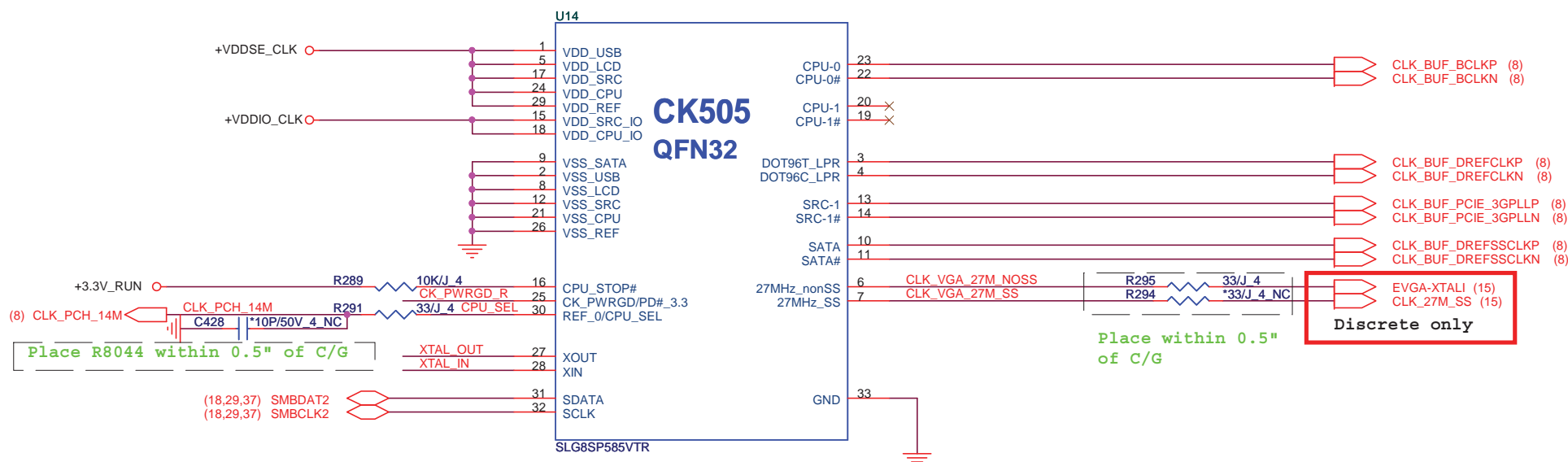


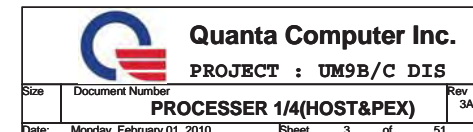
UM9B/C DISCRETE SYSTEM DIAGRAM



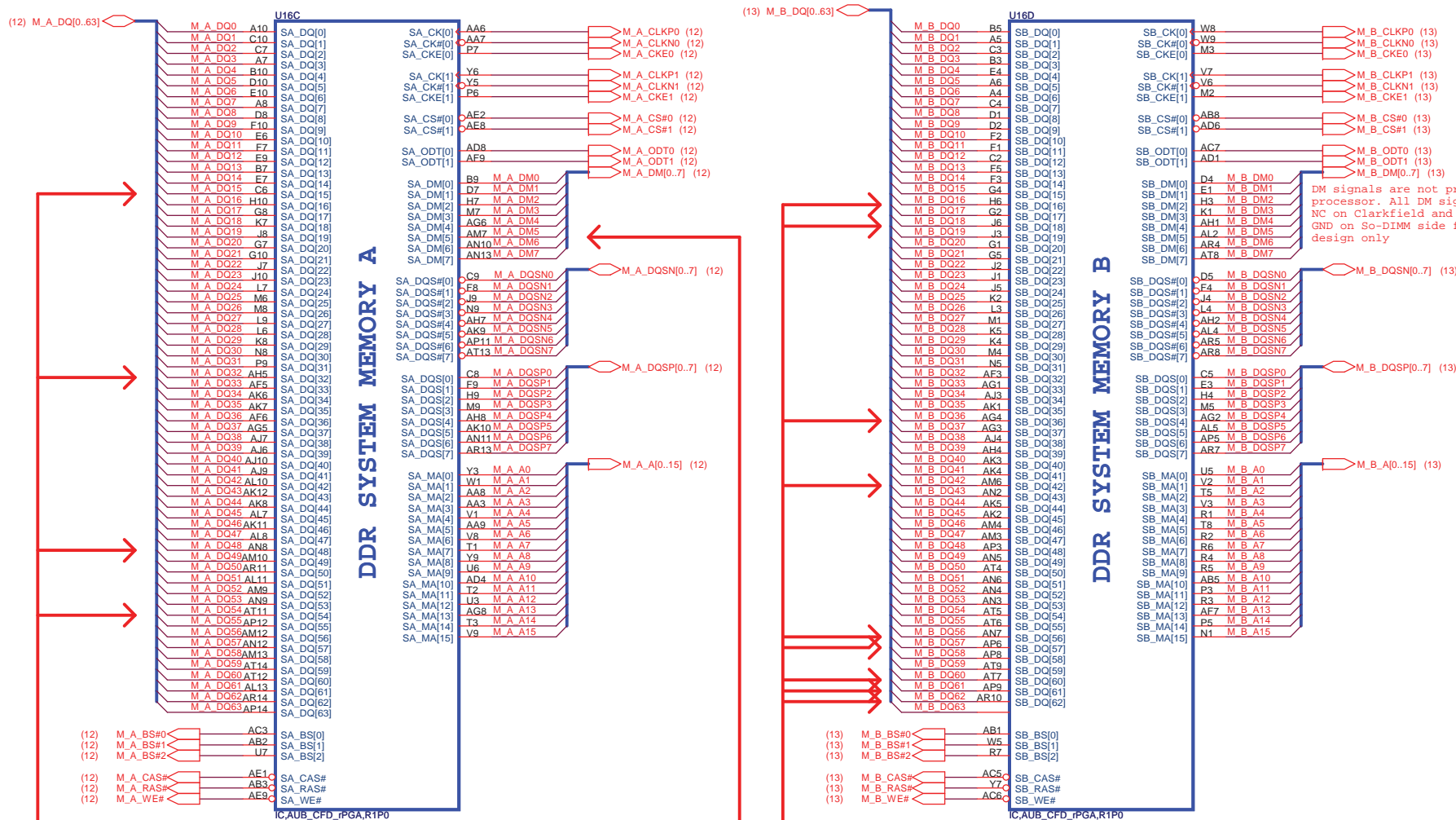


PDC (Power Cap quantities follow UM3)






AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.



Quanta Computer Inc.
PROJECT : UM9B/C DIS

Size	Document Number	Rev
	PROCESSOR 2/4(DDR)	3A
Date:	Monday, February 01, 2010	Sheet 4 of 51

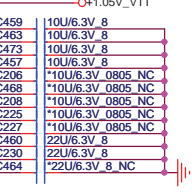
Name different with power

C477	*22U/6.3V 8 NC	AG35	VCC1
C479	*22U/6.3V 8 NC	AG34	VCC2
C501	*22U/6.3V 8 NC	AG32	VCC3
C472	*22U/6.3V 8 NC	AG31	VCC4
C203	*22U/6.3V 8 NC	AG30	VCC5
C202	22U/6.3V 8	AG29	VCC6
C470	22U/6.3V 8	AG28	VCC7
C469	22U/6.3V 8	AG27	VCC8
C499	22U/6.3V 8	AG26	VCC9
C214	22U/6.3V 8	AF35	VCC10
C204	22U/6.3V 8	AF34	VCC11
C504	22U/6.3V 8	AF32	VCC12
C500	*10U/6.3V 8 NC	AF33	VCC13
C200	*10U/6.3V 8 NC	AF31	VCC14
C205	*10U/6.3V 8 NC	AF30	VCC15
C476	*10U/6.3V 8 NC	AF29	VCC16
C213	10U/6.3V 8	AF28	VCC17
C201	10U/6.3V 8	AF27	VCC18
C478	10U/6.3V 8	AF26	VCC19
C217	10U/6.3V 8	AD35	VCC20
C219	10U/6.3V 8	AD34	VCC21
C471	10U/6.3V 8	AD33	VCC22
C218	10U/6.3V 8	AD32	VCC23
C503	10U/6.3V 8	AD31	VCC24
C475	10U/6.3V 8	AD30	VCC25
C215	10U/6.3V 8	AD29	VCC26
C502	10U/6.3V 8	AD28	VCC27
C216	10U/6.3V 8	AD27	VCC28
C196	*470U NC	AD26	VCC30
C191	*470U NC	AC35	VCC31
		AC34	VCC32
		AC33	VCC33
		AC32	VCC34
		AC31	VCC35
		AC30	VCC36
		AC29	VCC37
		AC28	VCC38
		AC27	VCC39
		AC26	VCC40
		AA35	VCC41
		AA34	VCC42
		AA33	VCC43
		AA32	VCC44
		AA31	VCC45
		AA30	VCC46
		AA29	VCC47
		AA28	VCC48
		AA27	VCC49
		AA26	VCC50
		Y35	VCC51
		Y34	VCC52
		Y33	VCC53
		Y32	VCC54
		Y31	VCC55
		Y30	VCC56
		Y29	VCC57
		Y28	VCC58
		Y27	VCC59
		Y26	VCC60
		V35	VCC61
		V34	VCC62
		V33	VCC63
		V32	VCC64
		V31	VCC65
		V30	VCC66
		V29	VCC67
		V28	VCC68
		V27	VCC69
		V26	VCC70
		U35	VCC71
		U34	VCC72
		U33	VCC73
		U32	VCC74
		U31	VCC75
		U30	VCC76
		U29	VCC77
		U28	VCC78
		U27	VCC79
		U26	VCC80
		R35	VCC81
		R34	VCC82
		R33	VCC83
		R32	VCC84
		R31	VCC85
		R30	VCC86
		R29	VCC87
		R28	VCC88
		R27	VCC89
		R26	VCC90
		P35	VCC91
		P34	VCC92
		P33	VCC93
		P32	VCC94
		P31	VCC95
		P30	VCC96
		P29	VCC97
		P27	VCC98
		P26	VCC99
			VCC100

U16F

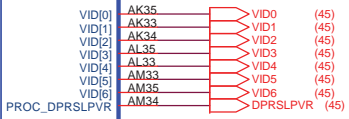
VTT0_1	AH14	C459	10U/6.3V 8
VTT0_2	AH12	C463	10U/6.3V 8
VTT0_3	AH11	C473	10U/6.3V 8
VTT0_4	AH10	C457	10U/6.3V 8
VTT0_5	J14	C206	*10U/6.3V 0805 NC
VTT0_6	J13	C468	*10U/6.3V 0805 NC
VTT0_7	H14	C208	*10U/6.3V 0805 NC
VTT0_8	AH12	C225	*10U/6.3V 0805 NC
VTT0_9	G14	C227	*10U/6.3V 0805 NC
VTT0_10	G13	G11	22U/6.3V 8
VTT0_11	G12	F14	22U/6.3V 8
VTT0_12	G11	E13	*22U/6.3V 8 NC
VTT0_13	F14	C464	
VTT0_14	E12		
VTT0_15	F11		
VTT0_16	F14		
VTT0_17	E12		
VTT0_18	D14		
VTT0_19	D13		
VTT0_20	D12		
VTT0_21	D11		
VTT0_22	D13		
VTT0_23	C14		
VTT0_24	C13		
VTT0_25	C12		
VTT0_26	B14		
VTT0_27	B12		
VTT0_28	A14		
VTT0_29	A13		
VTT0_30	A12		
VTT0_31	A11		
VTT0_32			
VTT0_33	AF10		
VTT0_34	AC10	C226	22U/6.3V 8
VTT0_35	AB10	C228	22U/6.3V 8
VTT0_36	Y10		
VTT0_37	W10		
VTT0_38	U10		
VTT0_39	T10		
VTT0_40	J12		
VTT0_41	J11		
VTT0_42	J16		
VTT0_43	J15		
VTT0_44			

18A

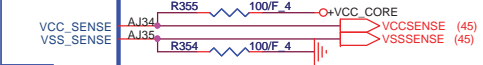
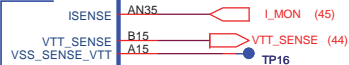


VTT Rail Values are
Auburndale VTT=1.05V
Clarkfield VTT=1.1V

PSI# AN33 H_PSI# (45)



H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V



IC_AUB_CFD_PGAR1P0

U16G

AT21	VAXG1
AT19	VAXG2
AT18	VAXG3
AT16	VAXG4
AR21	VAXG5
AR19	VAXG6
AR18	VAXG7
AP21	VAXG8
AP19	VAXG9
AP18	VAXG10
AP16	VAXG11
AN21	VAXG12
AN19	VAXG13
AN18	VAXG14
AM18	VAXG15
AM16	VAXG16
AM21	VAXG17
AM19	VAXG18
AM18	VAXG19
AL21	VAXG20
AL19	VAXG21
AL18	VAXG22
AL16	VAXG23
AK21	VAXG24
AK19	VAXG25
AK18	VAXG26
AK16	VAXG27
AJ21	VAXG28
AJ19	VAXG29
AJ18	VAXG30
AJ16	VAXG31
AH21	VAXG32
AH19	VAXG33
AH18	VAXG34
AH16	VAXG35
	VAXG36

GRAPHICS

POWER

FDI

PEG & DMI

SENSE LINES

GRAPHICS VIDS

DDR3 - 1.5V RAILS

1.1V

1.8V

VAXG_SENSE

GFX_VID[0]

GFX_VR_EN

VDDQ1

VDDQ2

VDDQ3

VDDQ4

VDDQ5

VDDQ6

VDDQ7

VDDQ8

VDDQ9

VDDQ10

VDDQ11

VDDQ12

VDDQ13

VDDQ14

VDDQ15

VDDQ16

VDDQ17

VDDQ18

VTT0_59

VTT0_60

VTT0_61

VTT0_62

VTT0_63

VTT1_64

VTT1_65

VTT1_66

VTT1_67

VTT1_68

VCCPLL1

VCCPLL2

VCCPLL3

L26

L27

M26

C199

C198

C481

C197

C480

C234

C233

C232

C235

C237

C238

C236

C239

C231

C230

C229

C228

C227

C226

C225

C224

C223

C222

C221

C220

C219

C218

C217

C216

C215

C214

C213

C212

C211

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C177

C176

C175

C174

C173

C172

C171

C170

C169

C168

C167

C166

C165

C164

C163

C162

C161

C160

C159

C158

C157

C156

C155

C154

C153

C152

C151

C150

C149

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C146

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C144

C143

C142

C141

C140

C139

C138

C137

C136

C135

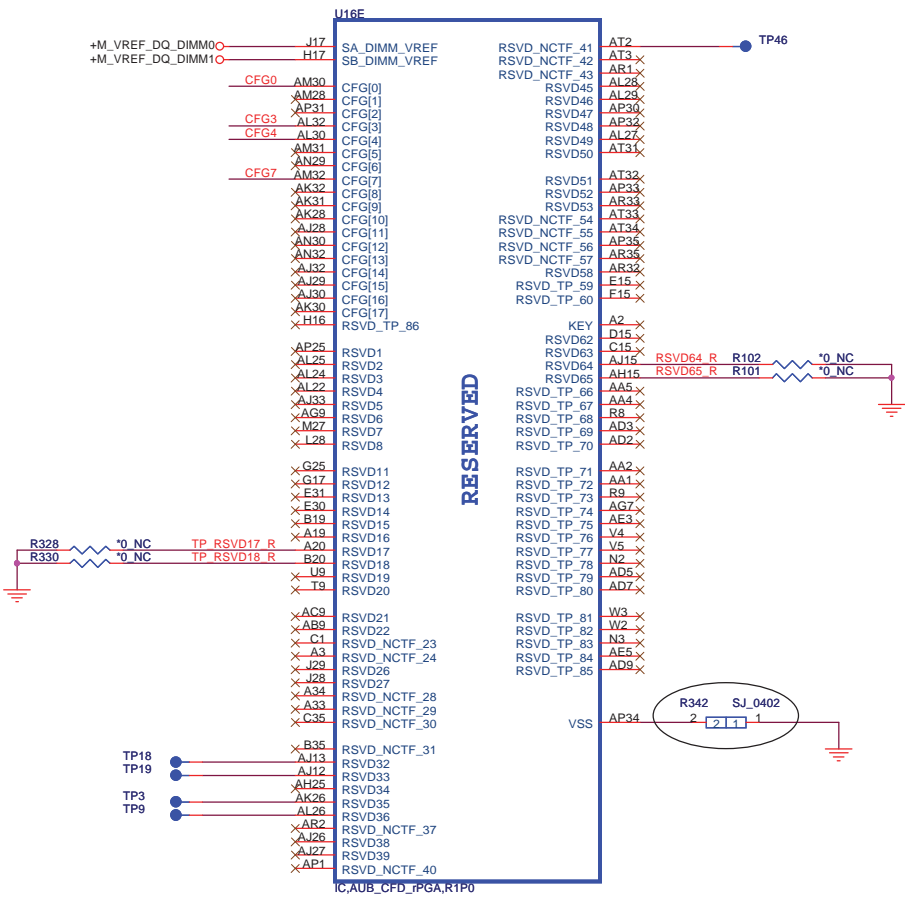
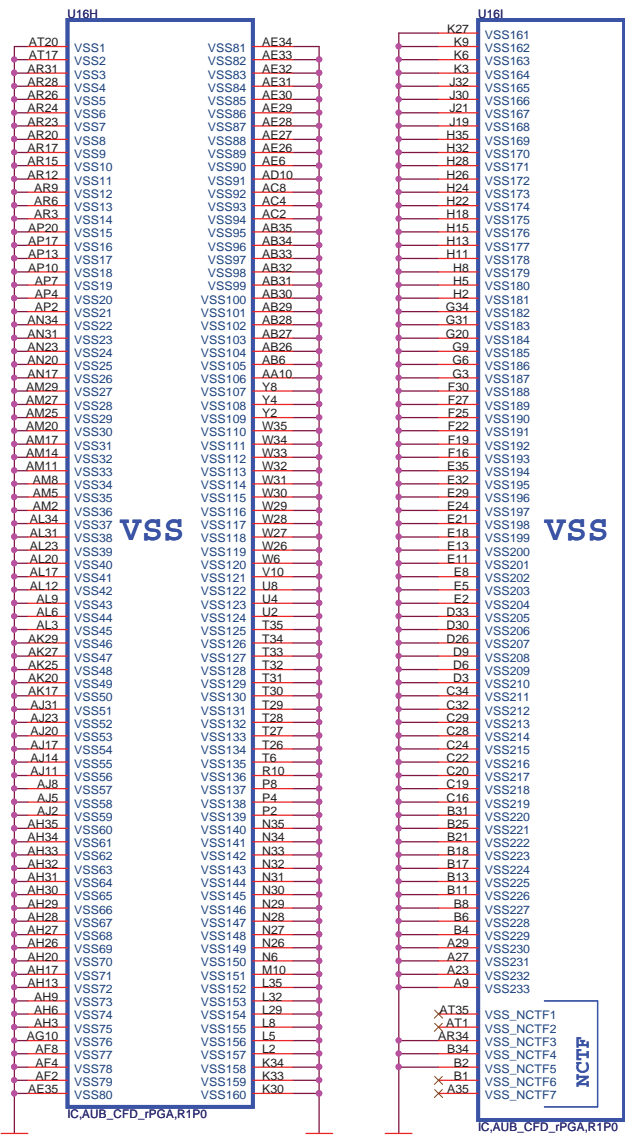
C134

C133

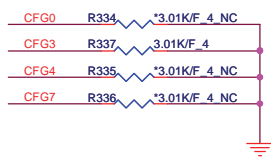
C132

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)




The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

For Discrete only

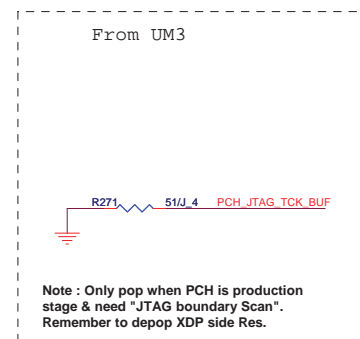
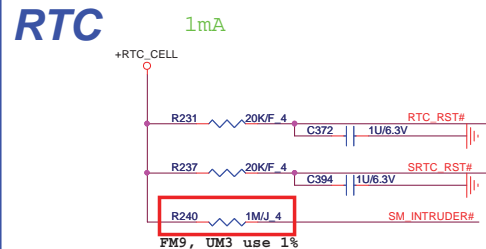
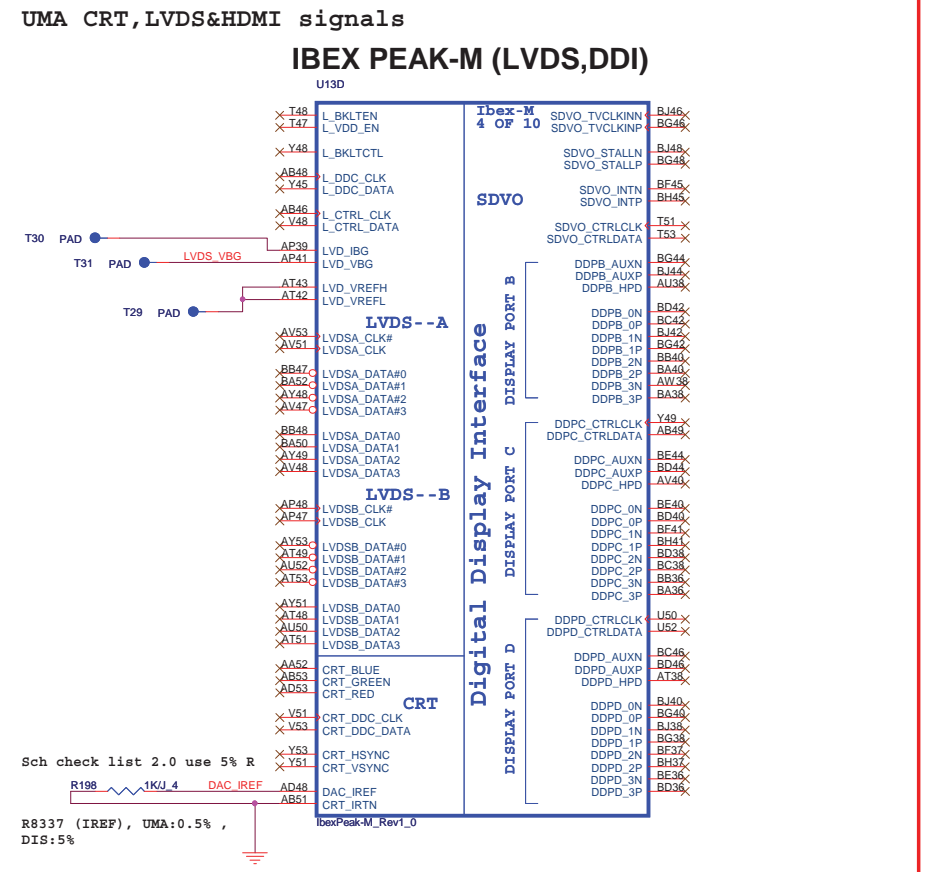
CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG



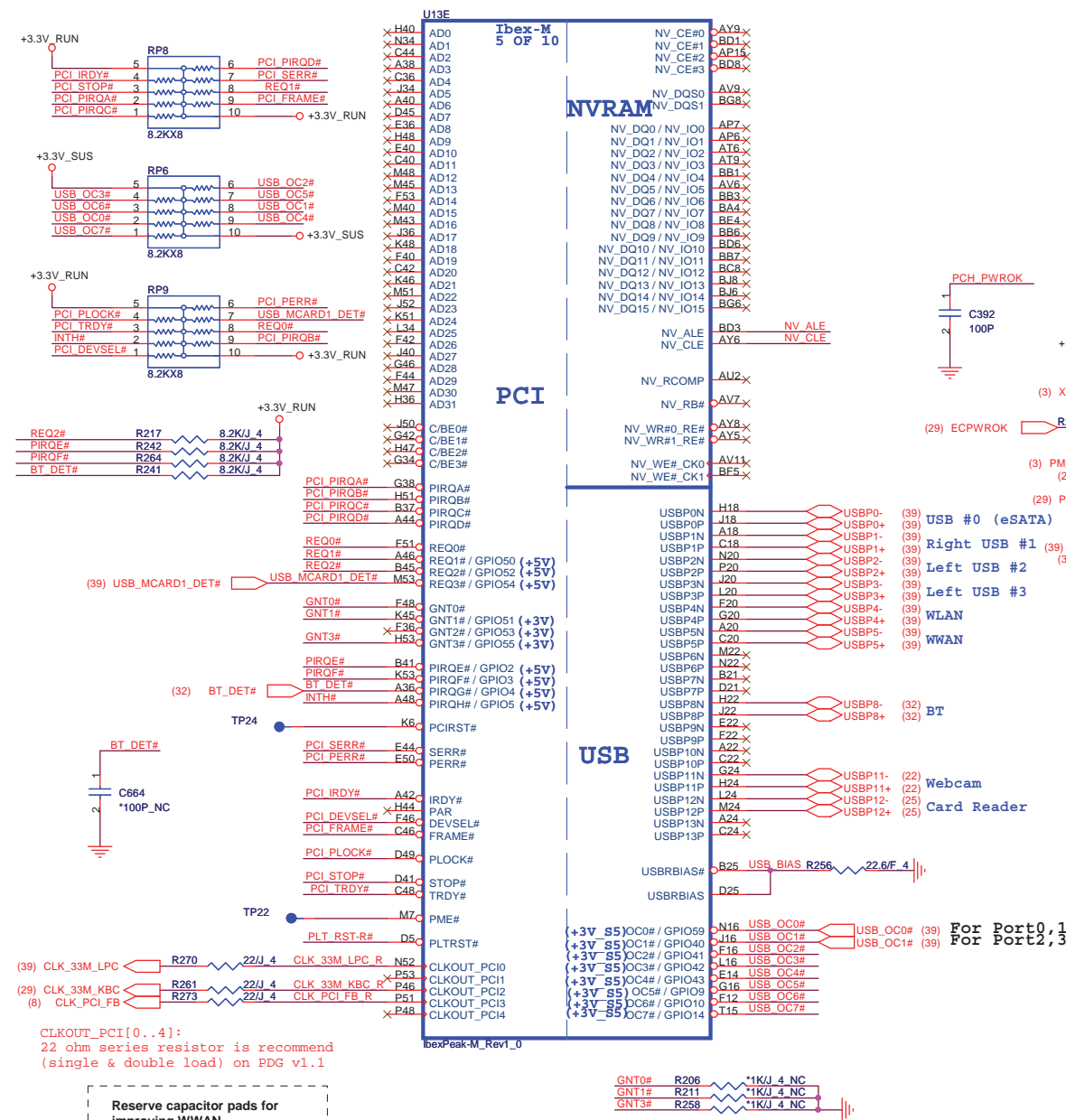
Quanta Computer Inc.
PROJECT : UM9B/C DIS

Size Document Number
PROCESSOR 4/4 (GND)

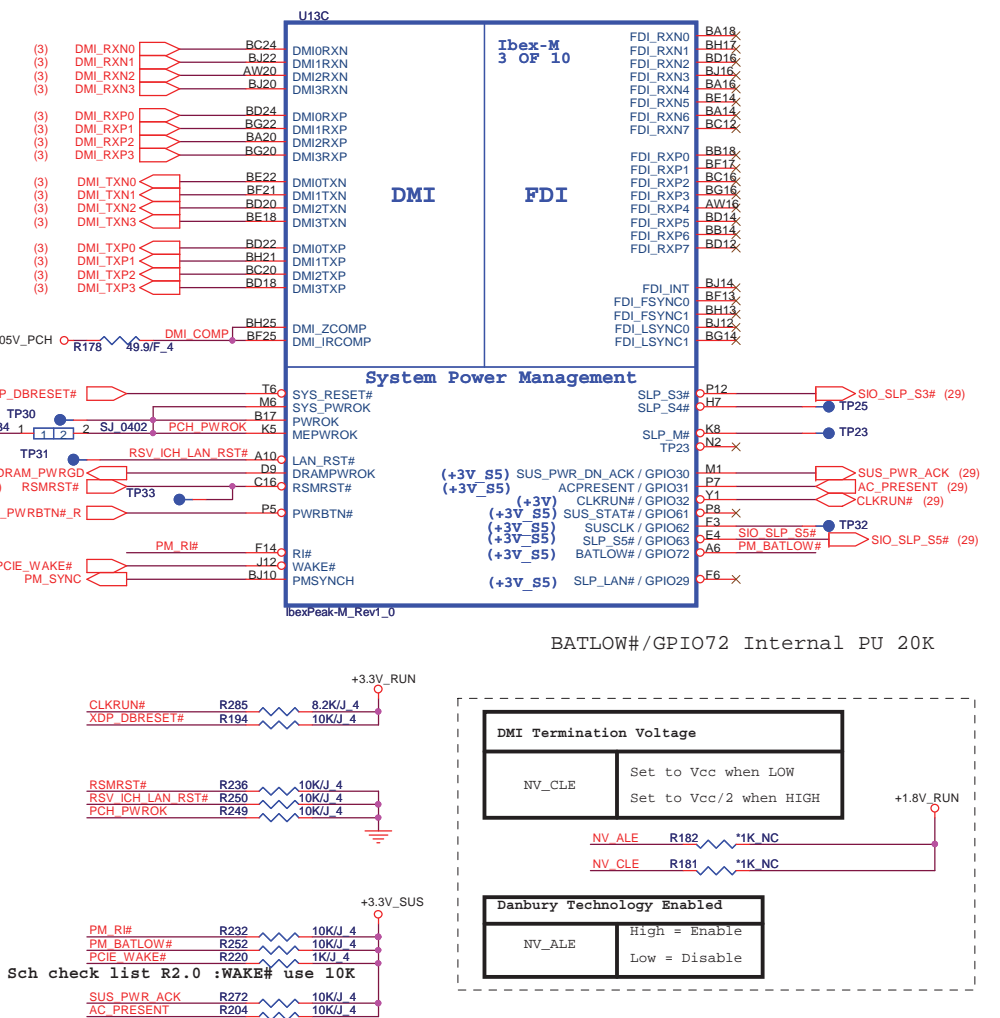
Date: Wednesday, January 27, 2010 Sheet 6 of 51



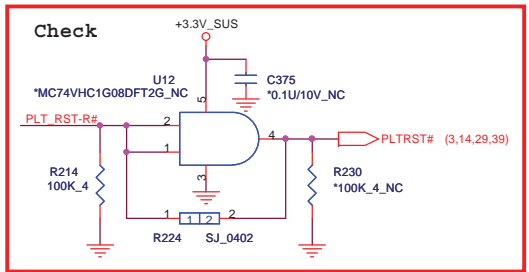
IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (DMI,FDI,GPIO)



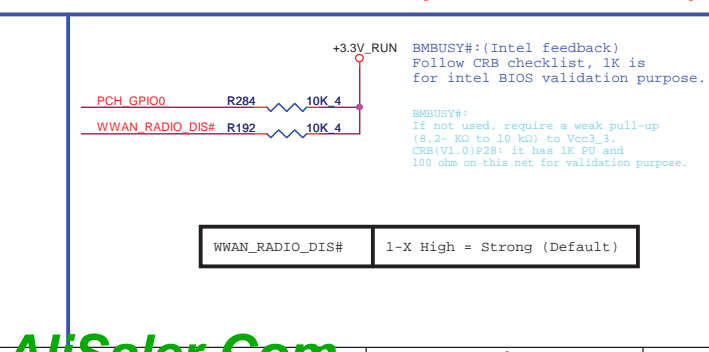
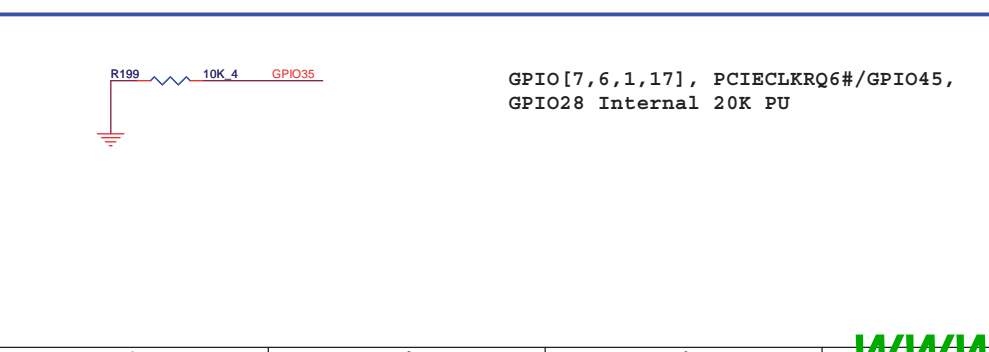
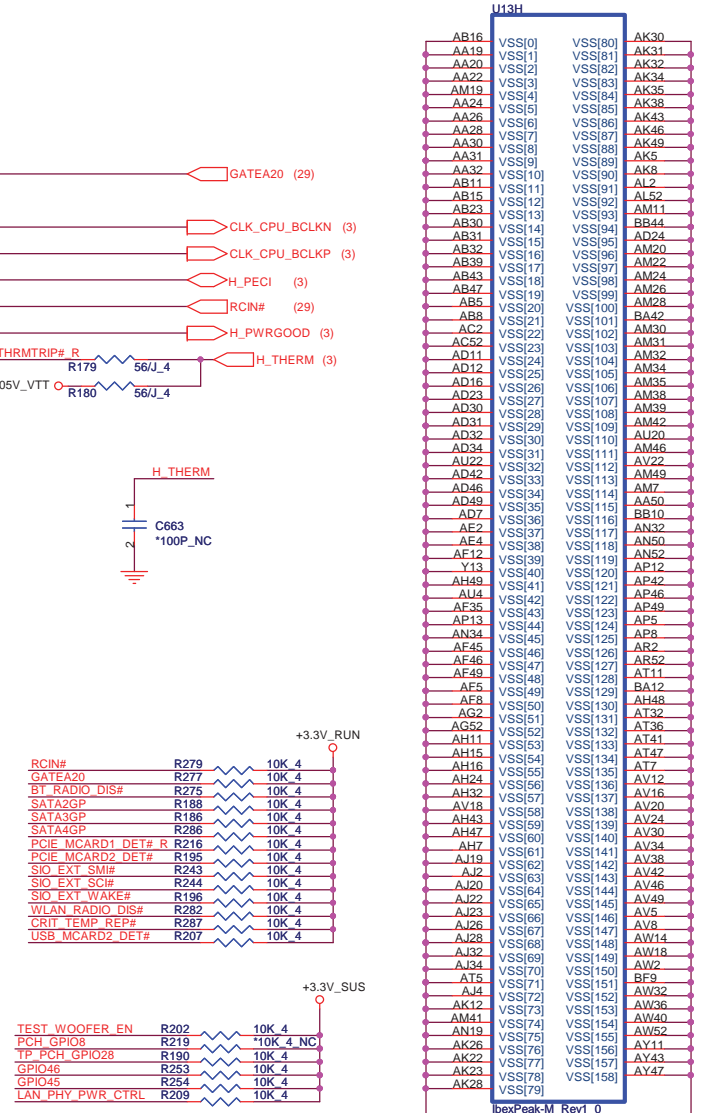
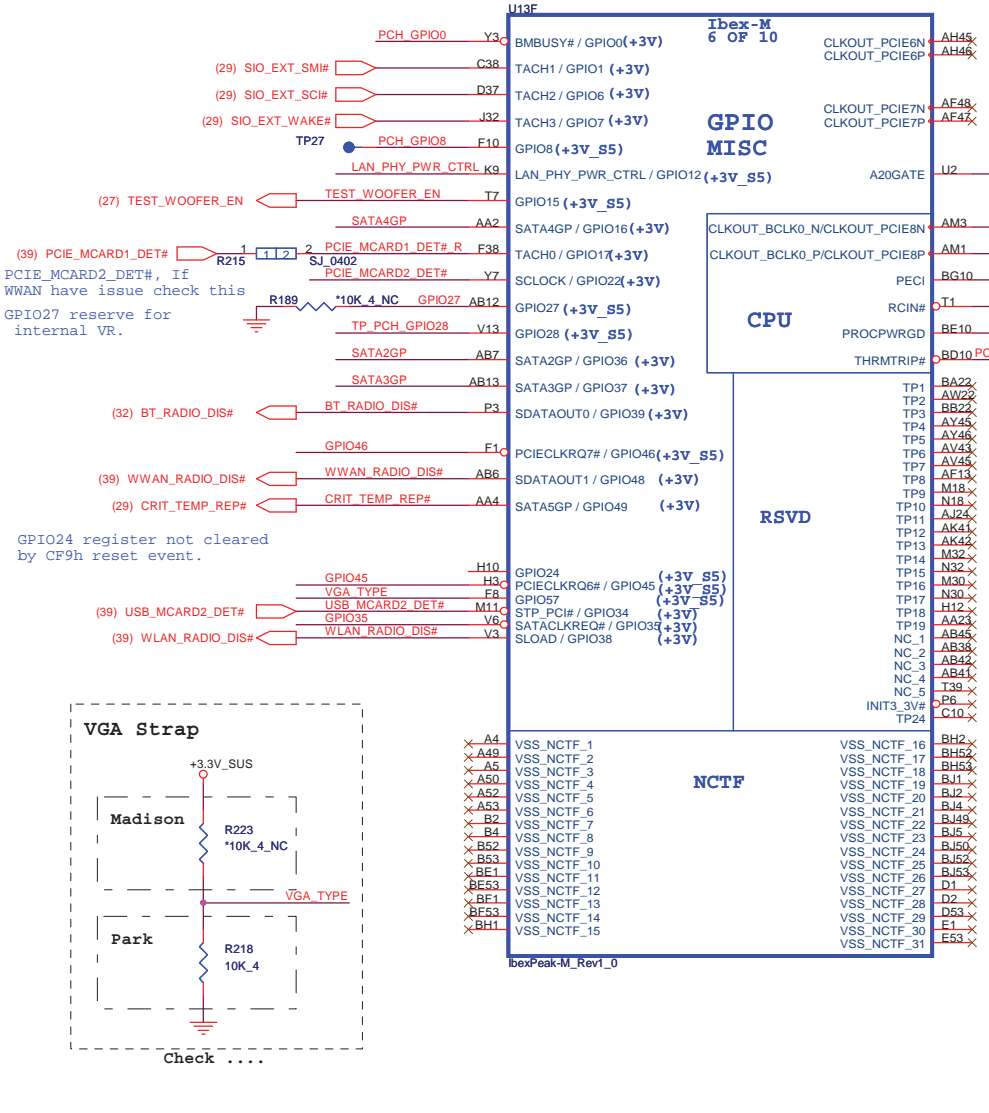
BATLOW#/GPIO72 Internal PU 20K



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

10



Flash Descriptor Security Override

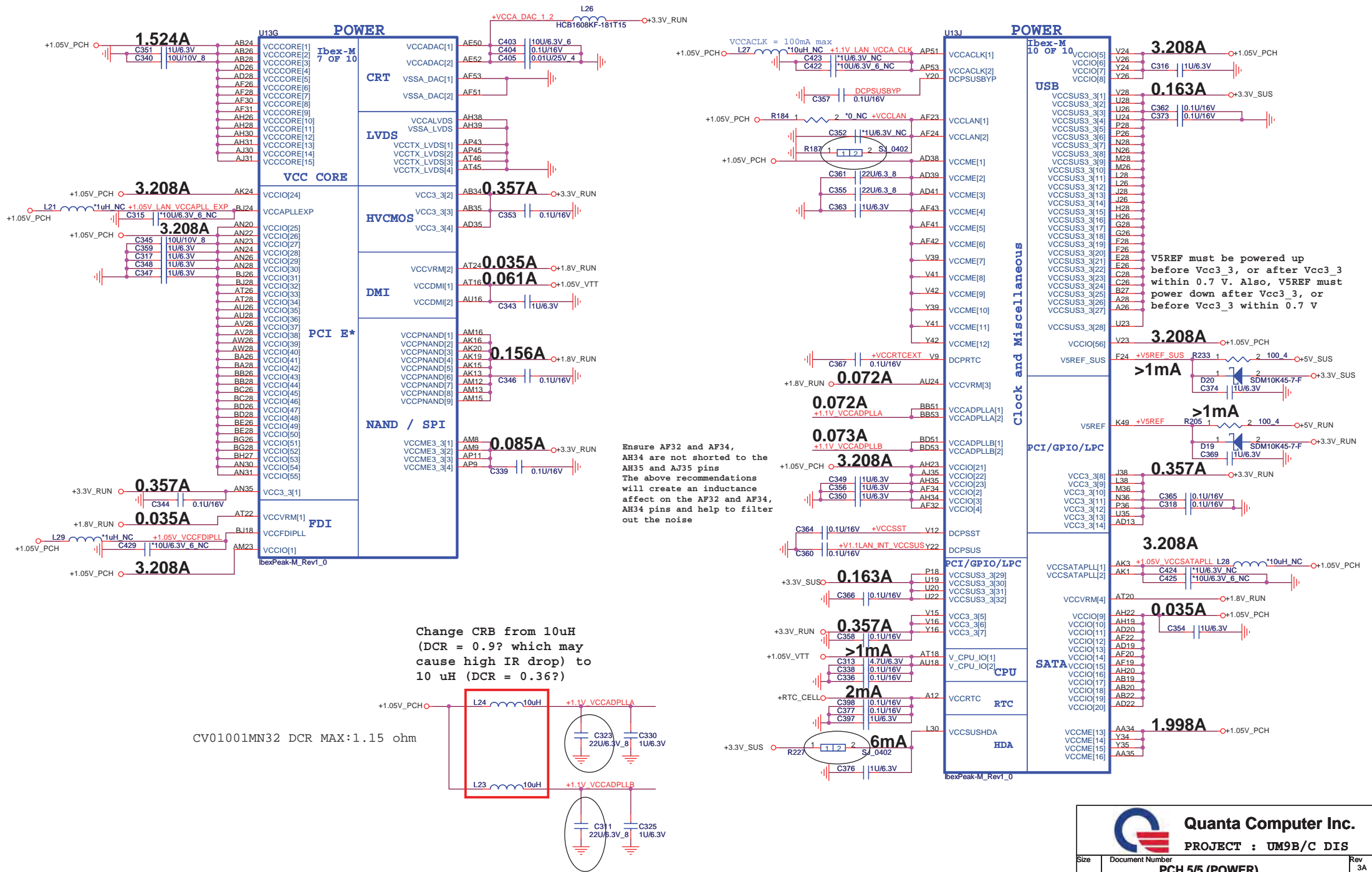
GPIO33	Low = Enabled High = Disabled
--------	----------------------------------

(7,29) PCH_MELOCK R197 1KJ_4_NC

(Internal 20K/F pull high to +3.3V_RUN)

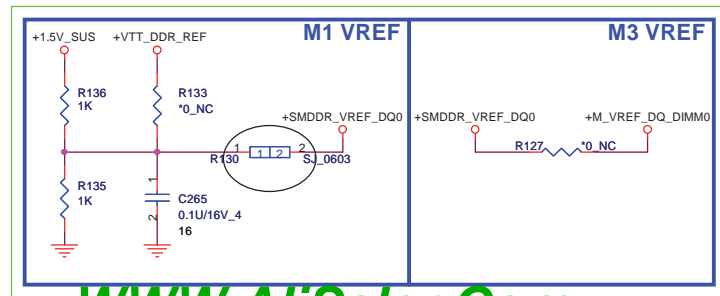
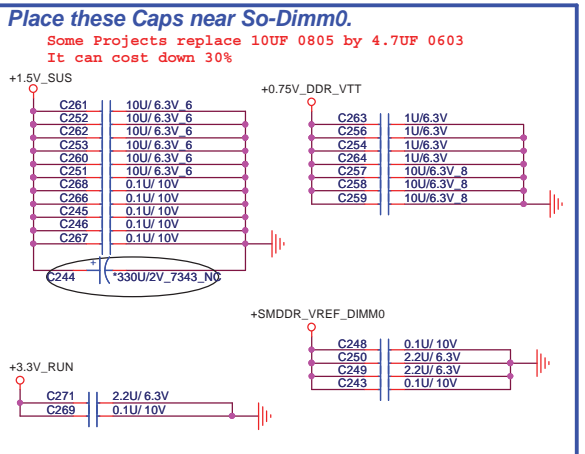
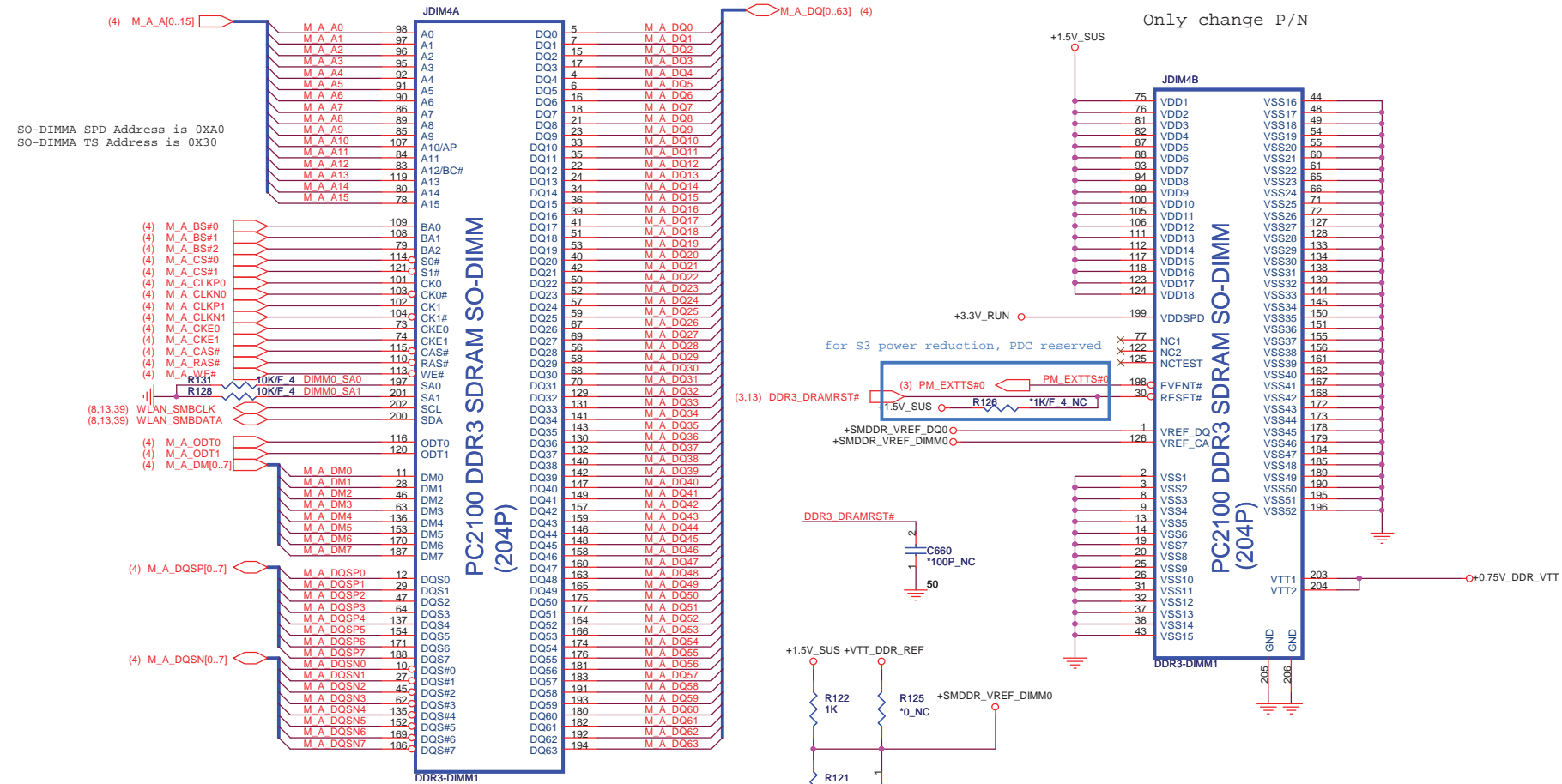
Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

WWAN_RADIO_DIS#	1-X High = Strong (Default)
-----------------	-----------------------------




Only change P/N

Only change P/N



Quantities and M1/M3 follow UM3
Locations follow PDC

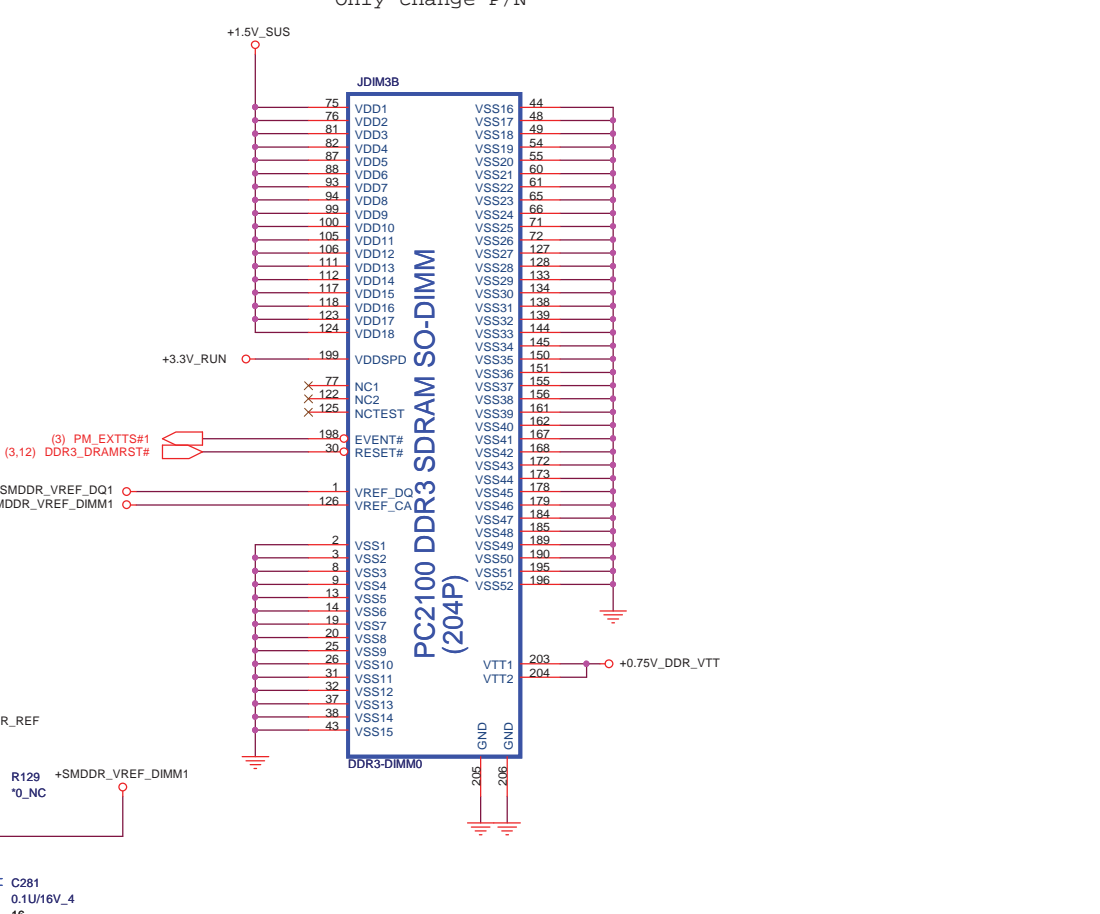
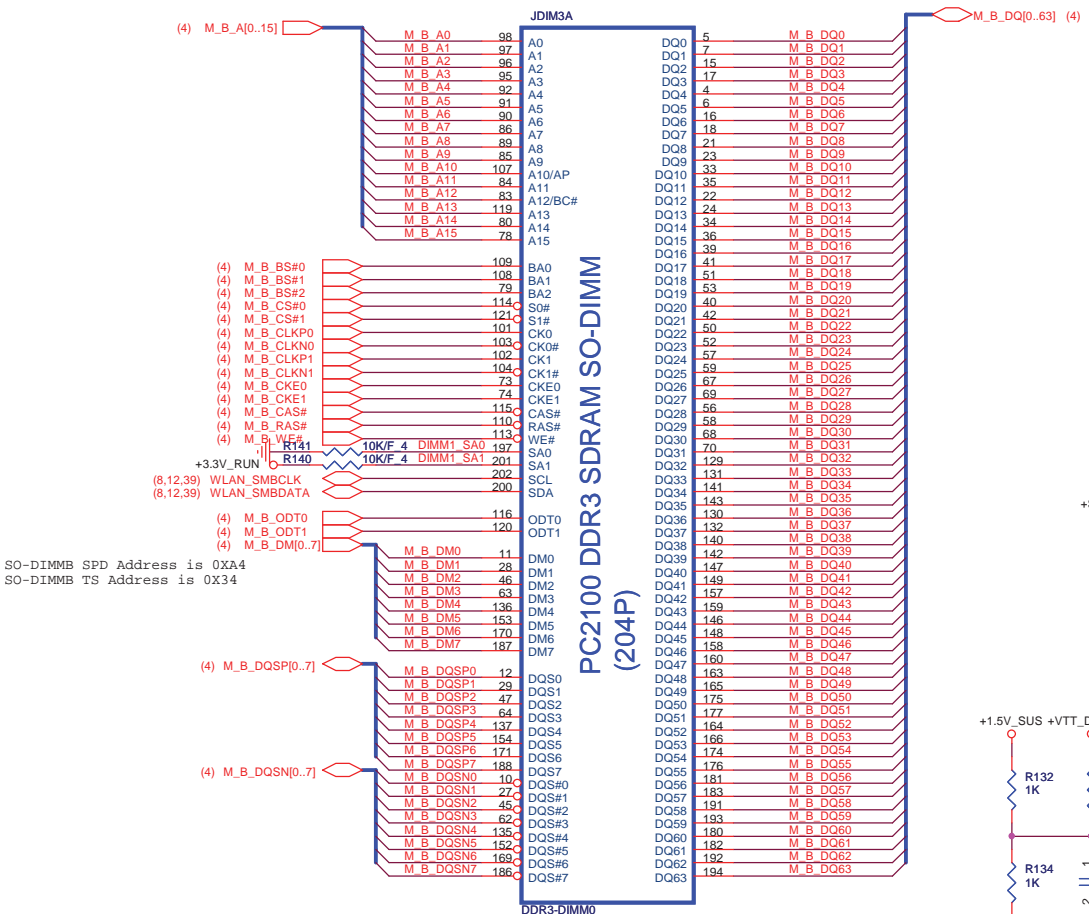


Quanta Computer Inc.
PROJECT : UM9B/C DIS

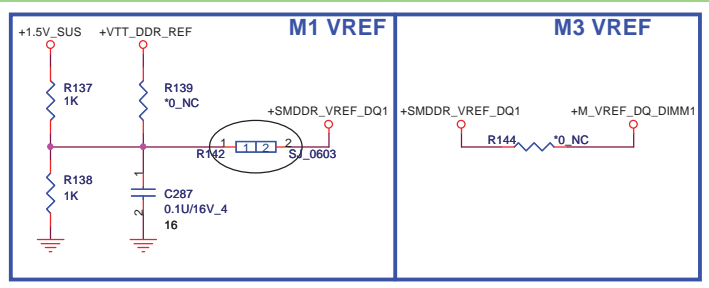
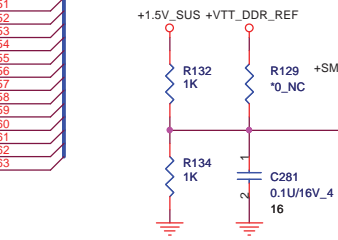
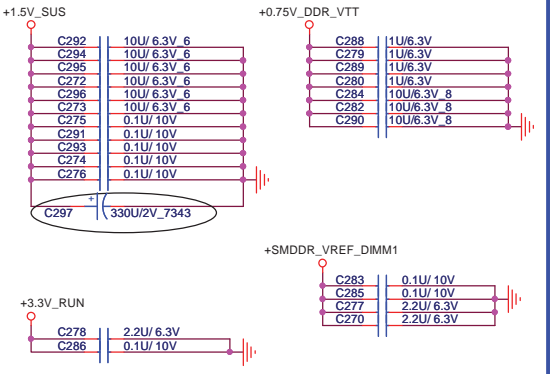
Size	Document Number	Rev
	DDR3 DIMM-0	3A
Date:	Monday, February 01, 2010	Sheet 12 of 51

Only change P/N


Only change P/N



Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



Quantities and M1/M3 follow UM3
Locations follow PDC

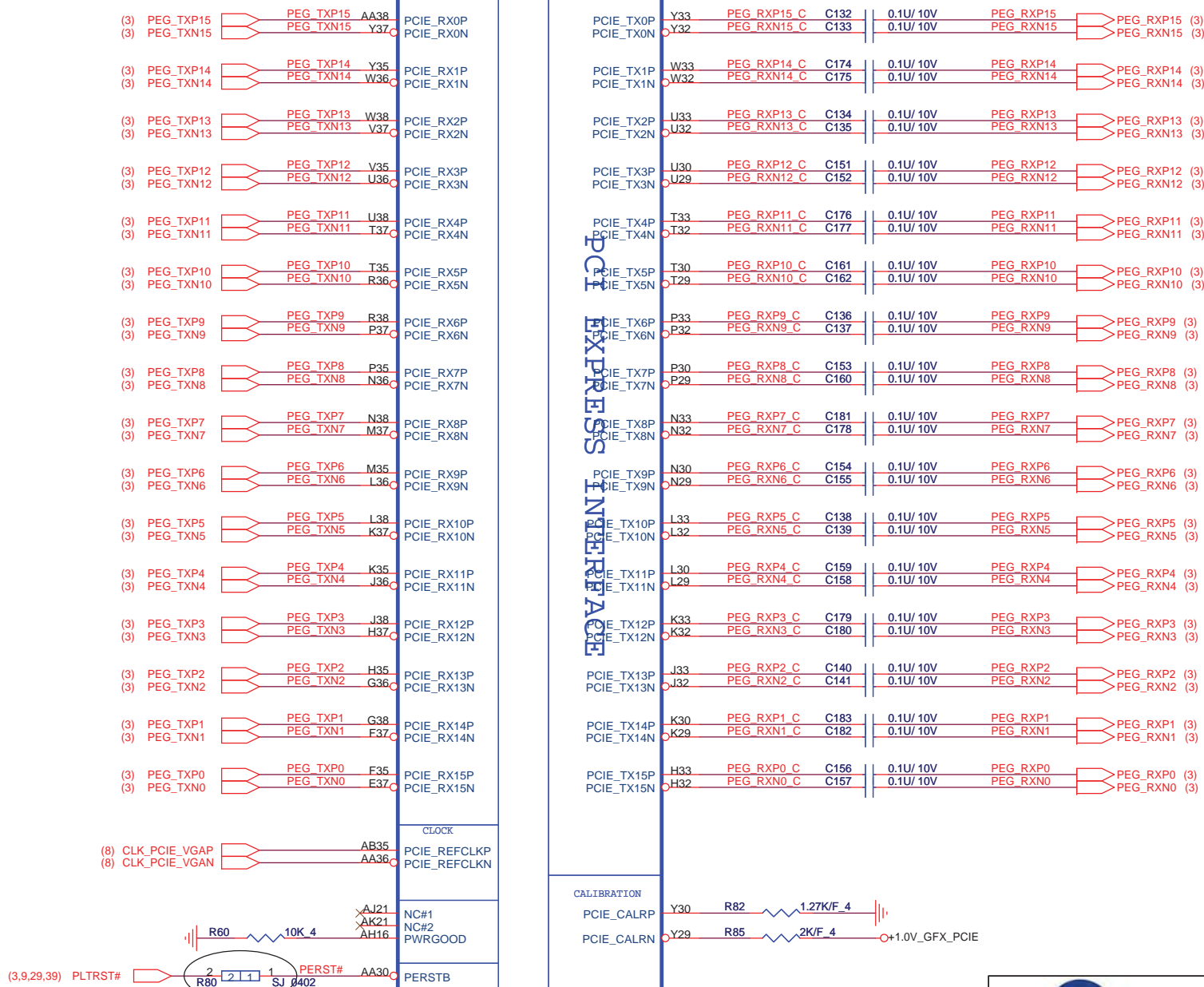


Quanta Computer Inc.
PROJECT : UM9B/C DIS

Size	Document Number	Rev
	DDR3 DIMM-1	3A
Date:	Monday, February 01, 2010	Sheet 13 of 51

U19A

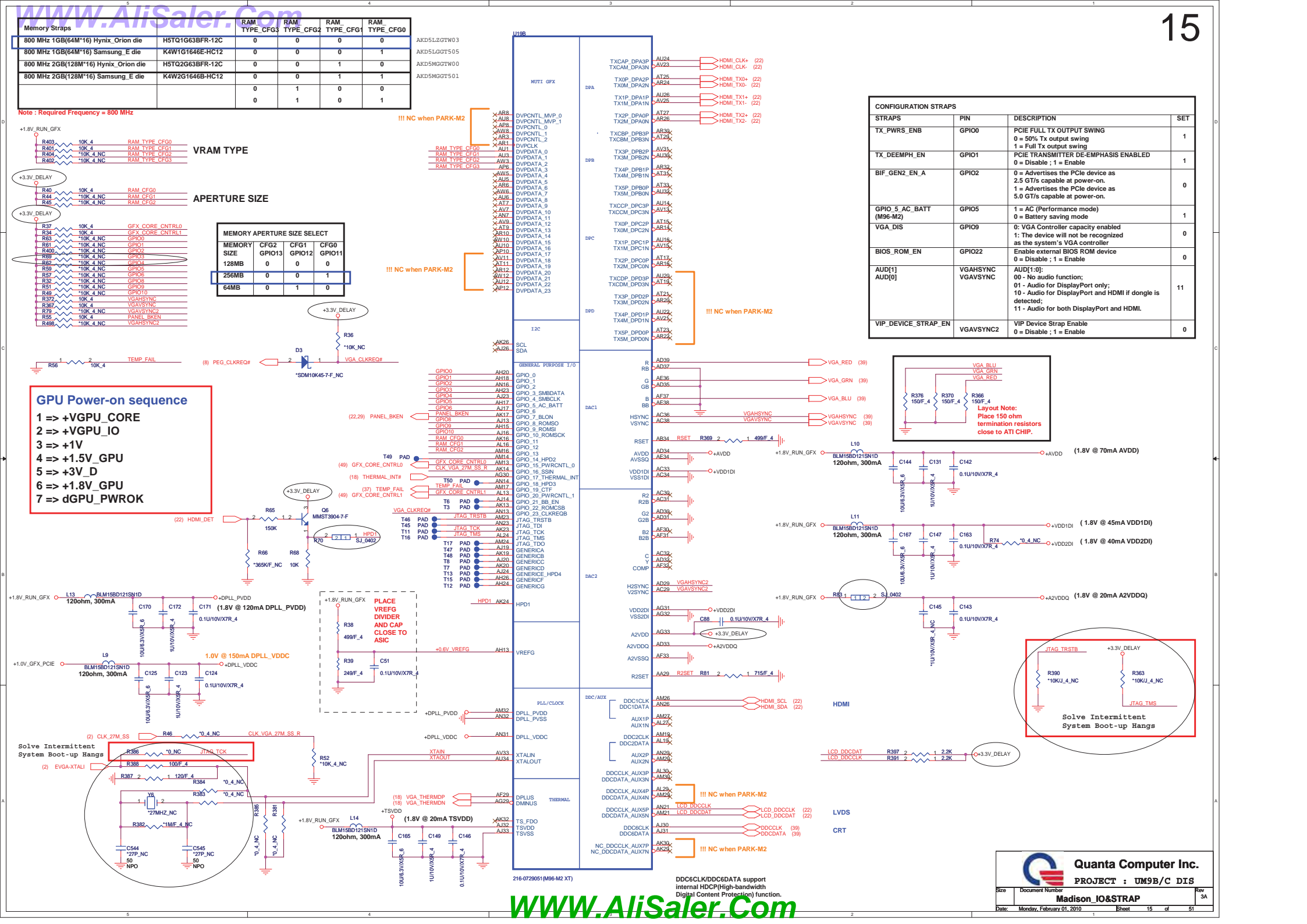
PCI EXPRESS INTERFACE

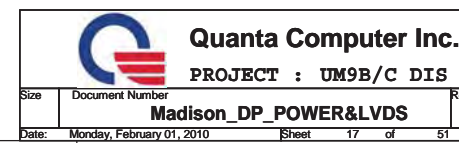


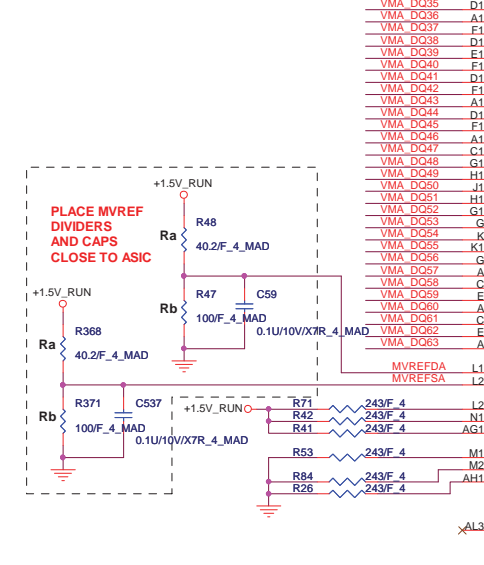
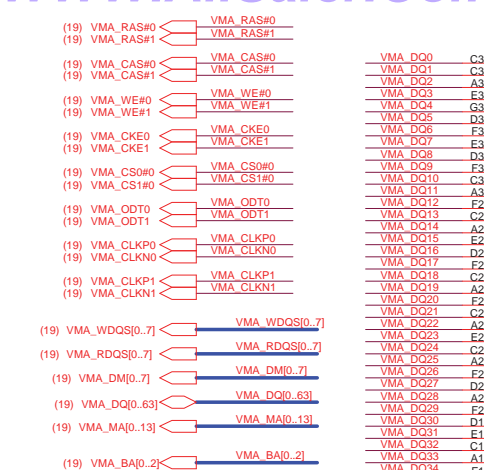
216-0729051(M96-M2 XT)

Quanta Computer Inc.
PROJECT : UM9B/C DIS

Size	Document Number	Rev
	Monday, February 01, 2010	3A
Madison PCIE I/F		
Sheet	14	of 51



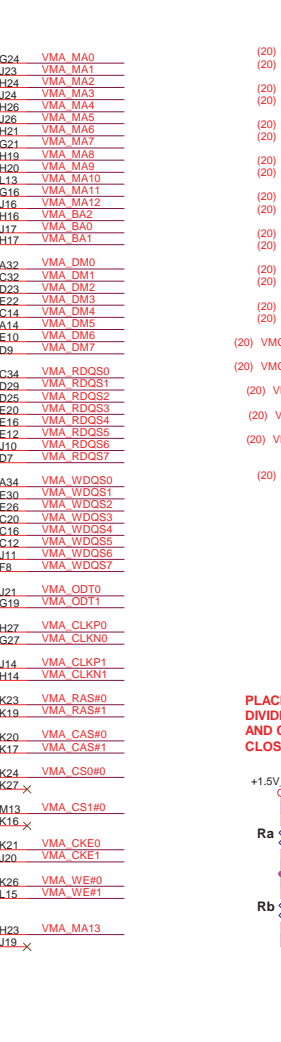
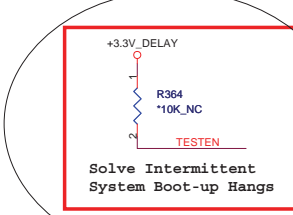




216-0729051(M96-M2 XT)

Solve Intermittent System Boot-up Hangs

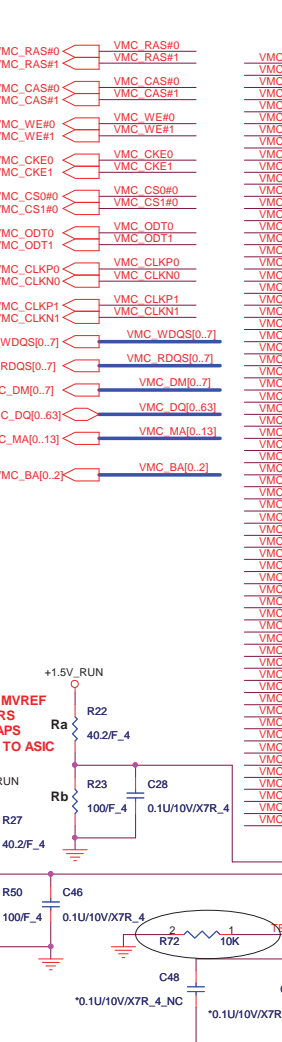
VGA	ENG	MP
R386	V	
R390	V	
R363	V	
R364	V	
R72		V



216-0729051(M96-M2 XT)

DDR3/GDDR3 Memory Stuff Option

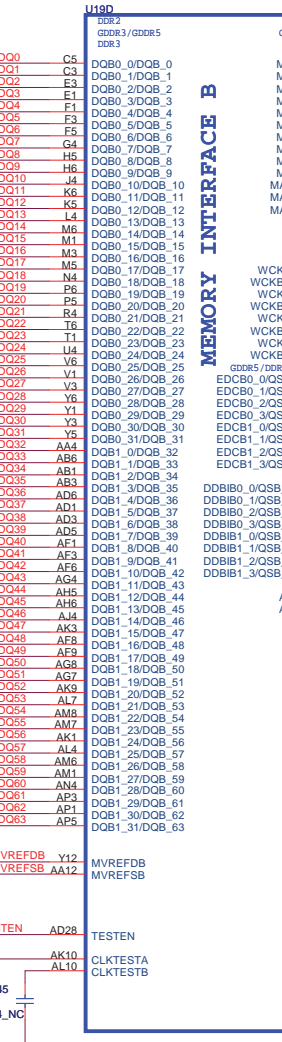
	GDDR3	DDR3
MVDDQ	1.5V/1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R



216-0729051(M96-M2 XT)

DDR3/GDDR3 Memory Stuff Option

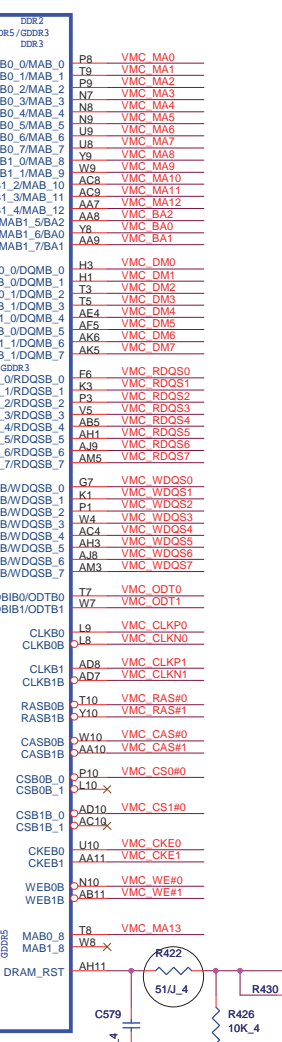
	GDDR3	DDR3
MVDDQ	1.5V/1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R



216-0729051(M96-M2 XT)

DDR3/GDDR3 Memory Stuff Option

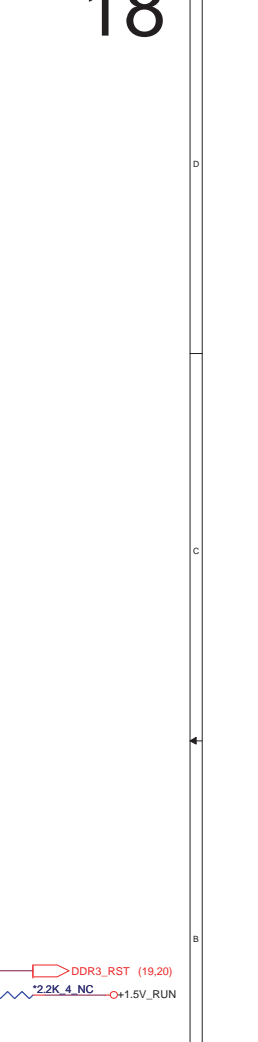
	GDDR3	DDR3
MVDDQ	1.5V/1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R



216-0729051(M96-M2 XT)

DDR3/GDDR3 Memory Stuff Option

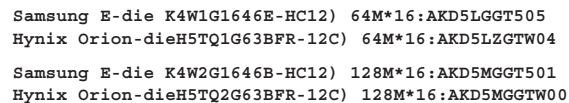
	GDDR3	DDR3
MVDDQ	1.5V/1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R



216-0729051(M96-M2 XT)

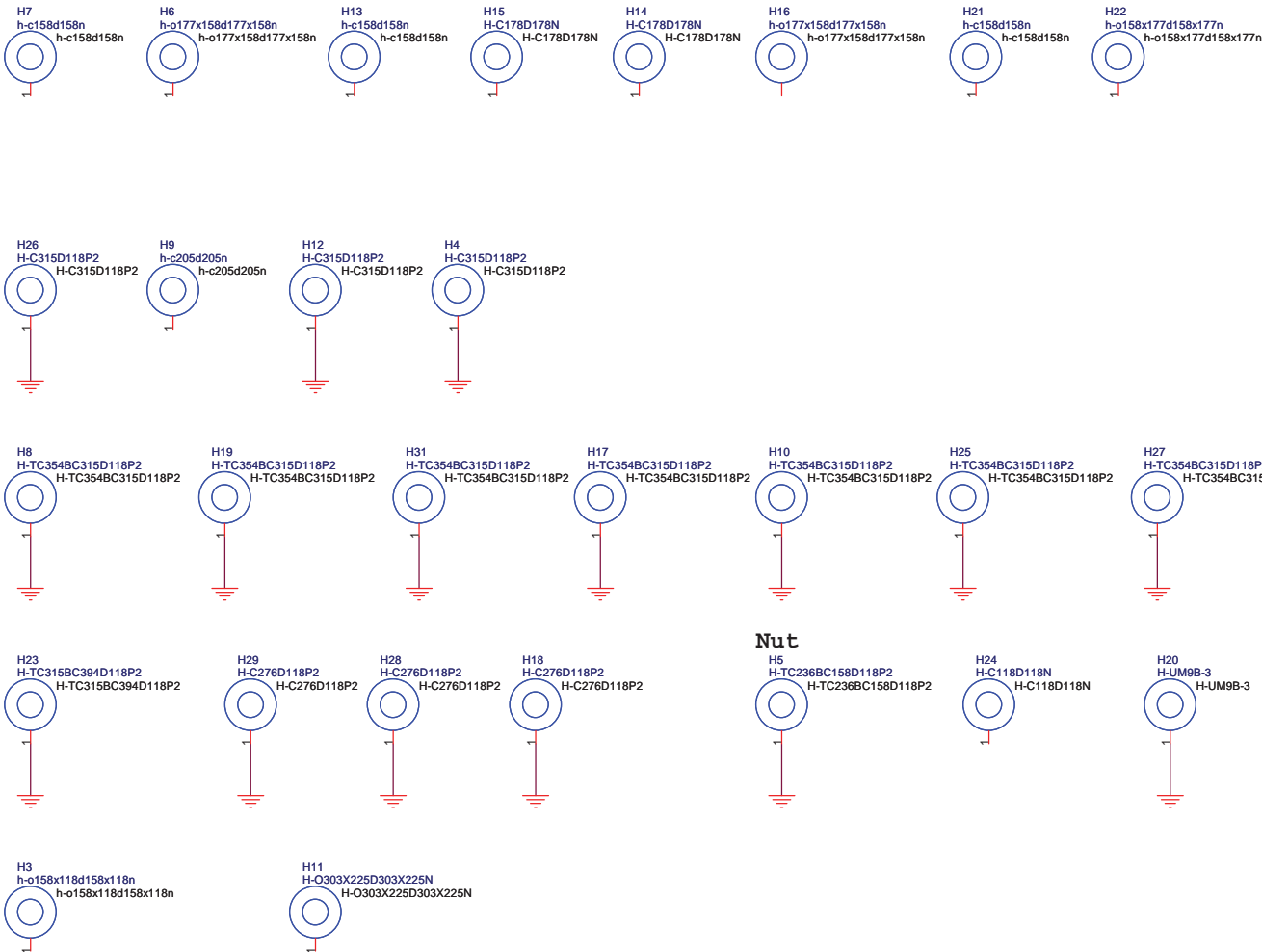
DDR3/GDDR3 Memory Stuff Option

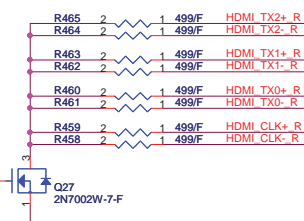
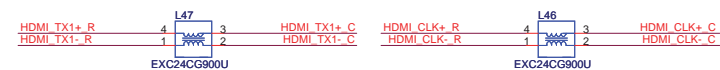
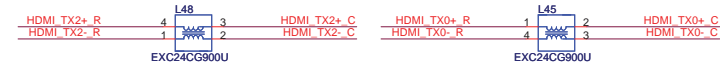
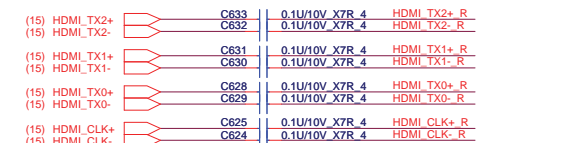
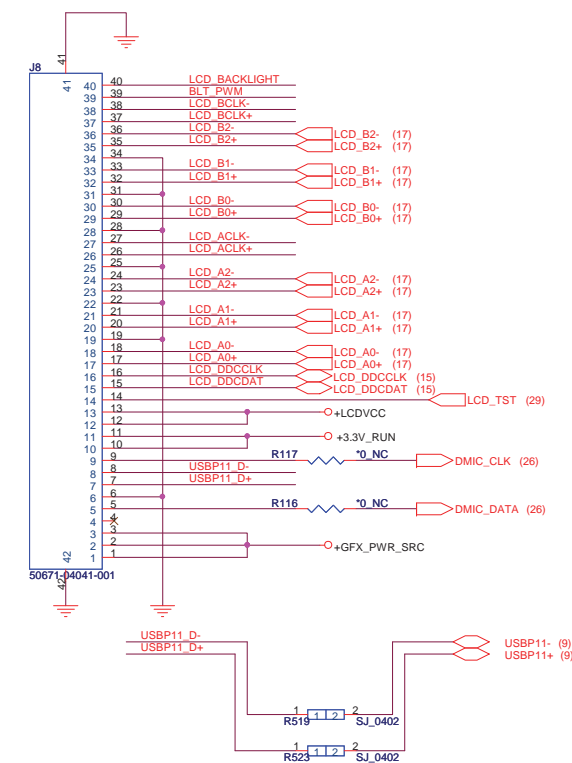
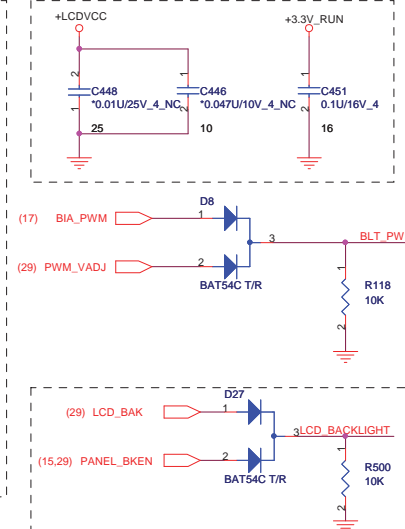
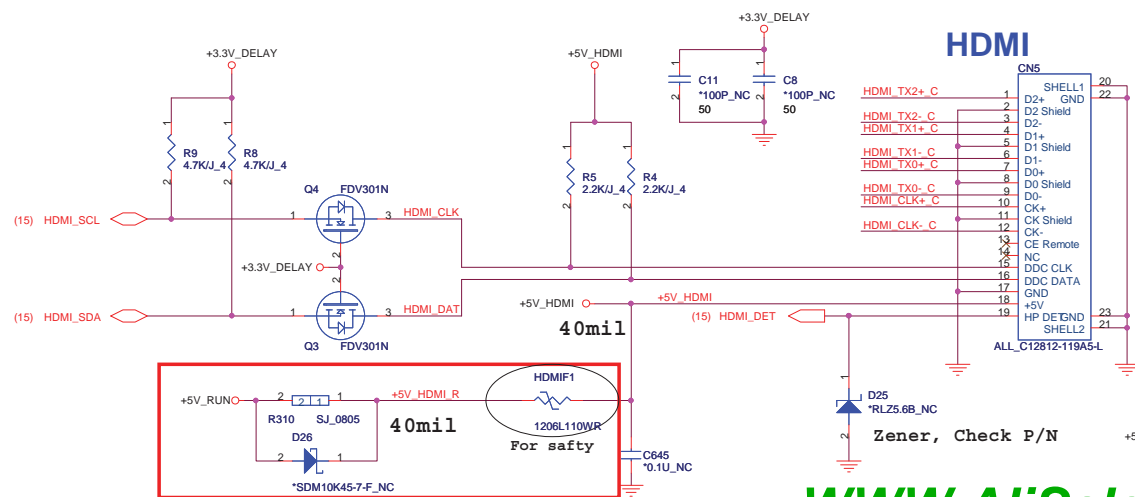
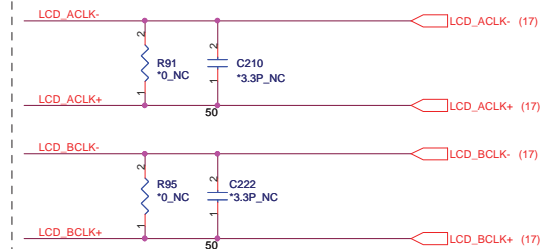
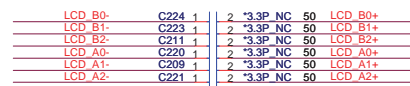
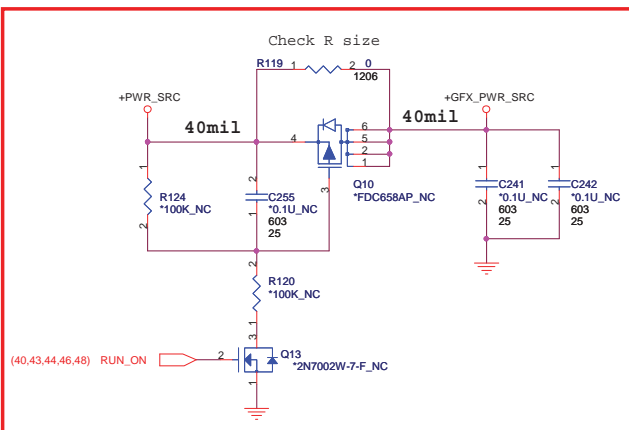
	GDDR3	DDR3
MVDDQ	1.5V/1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R







Follow 9/9 mail, check GND.

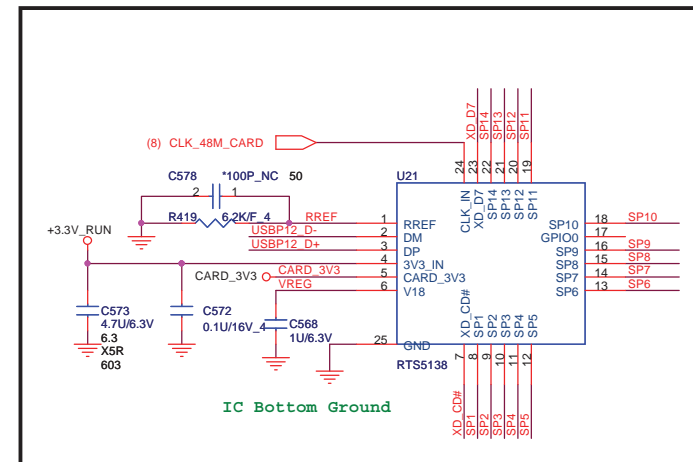
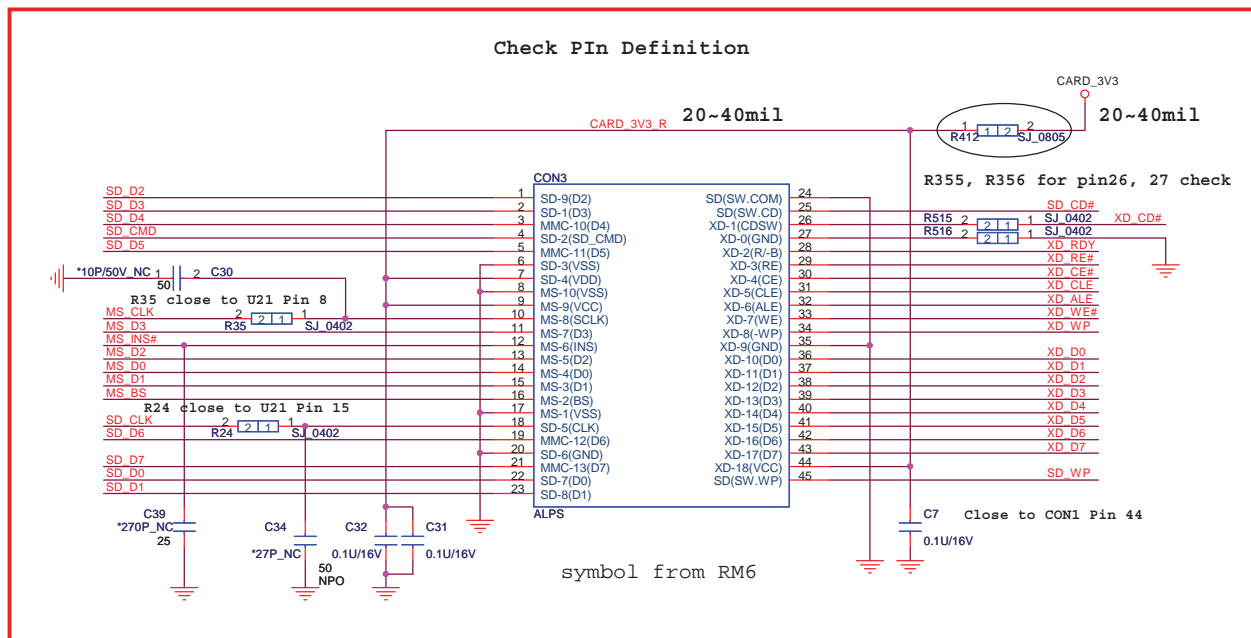




		Quanta Computer Inc.	
		PROJECT : UM9B/C DIS	
Size	Document Number		Rev
	CRT CONN		3A
Date:	Wednesday, January 27, 2010		Sheet 23 of 51

		Quanta Computer Inc.	
		PROJECT : UM9B/C DIS	
Size	Document Number		Rev
	DB CONN/Left USB		3A
Date:	Wednesday, January 27, 2010	Sheet	24 of 51

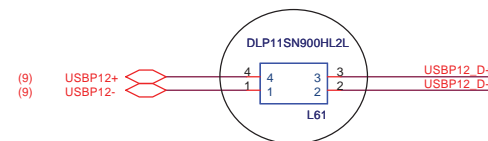
Check PIn Definition

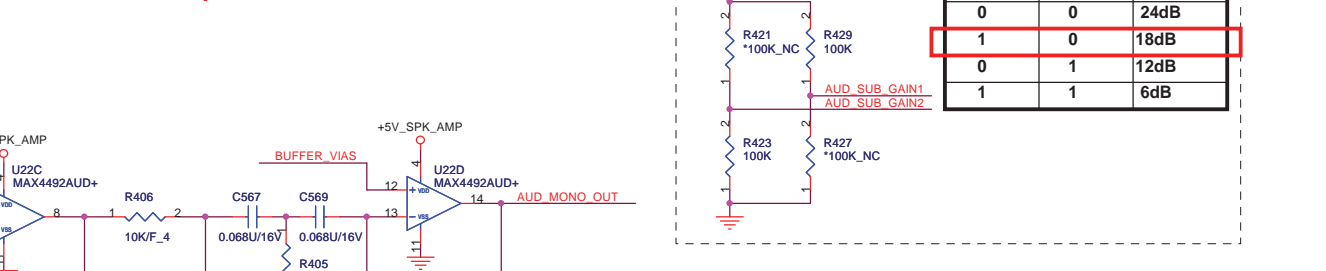
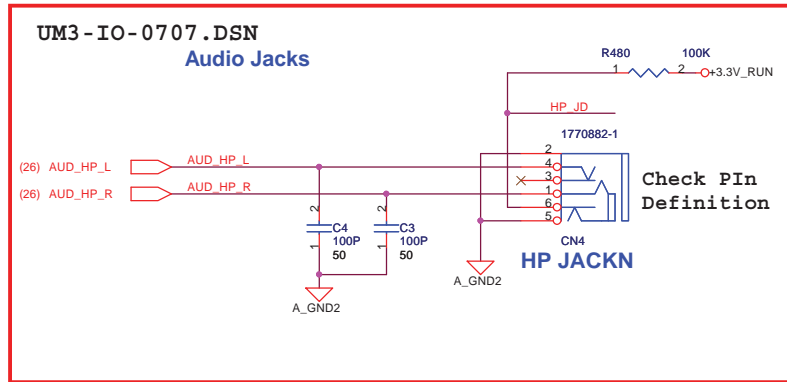


RTS5138-QFN24

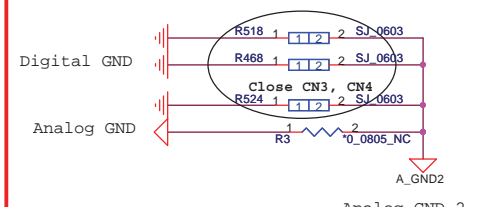
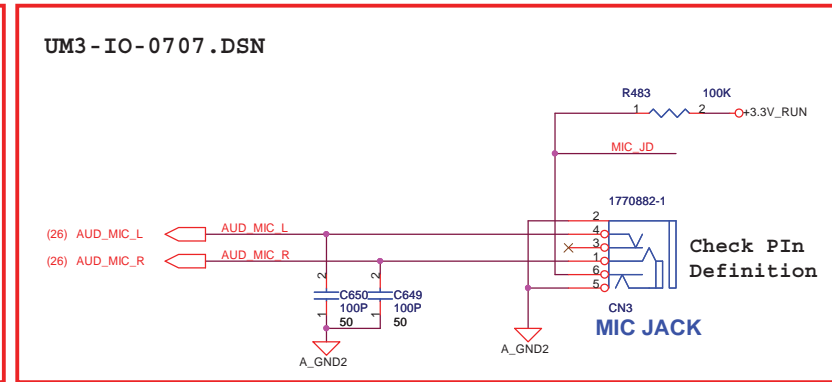
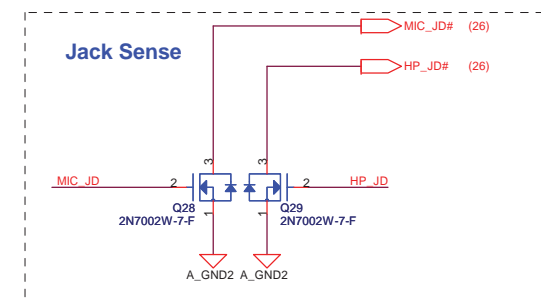
SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#	SD D1	MS INS#
SP3	XD CE#	SD D0	MS D3
SP4	XD CLE	SD D7	MS D7
SP5	XD ALE	SD D6	MS D6
SP6	XD WE#	SD CD#	MS D5
SP7	XD WP	SD D6	MS D6
SP8	XD D0	SD CLK	MS D2
SP9	XD D1	SD D5	MS D0
SP10	XD D2	SD CMD	MS D4
SP11	XD D3	SD D4	MS D1
SP12	XD D4	SD D3	MS D5
SP13	XD D5	SD D2	MS BS
SP14	XD D6	SD D1	MS BS

Share Pin

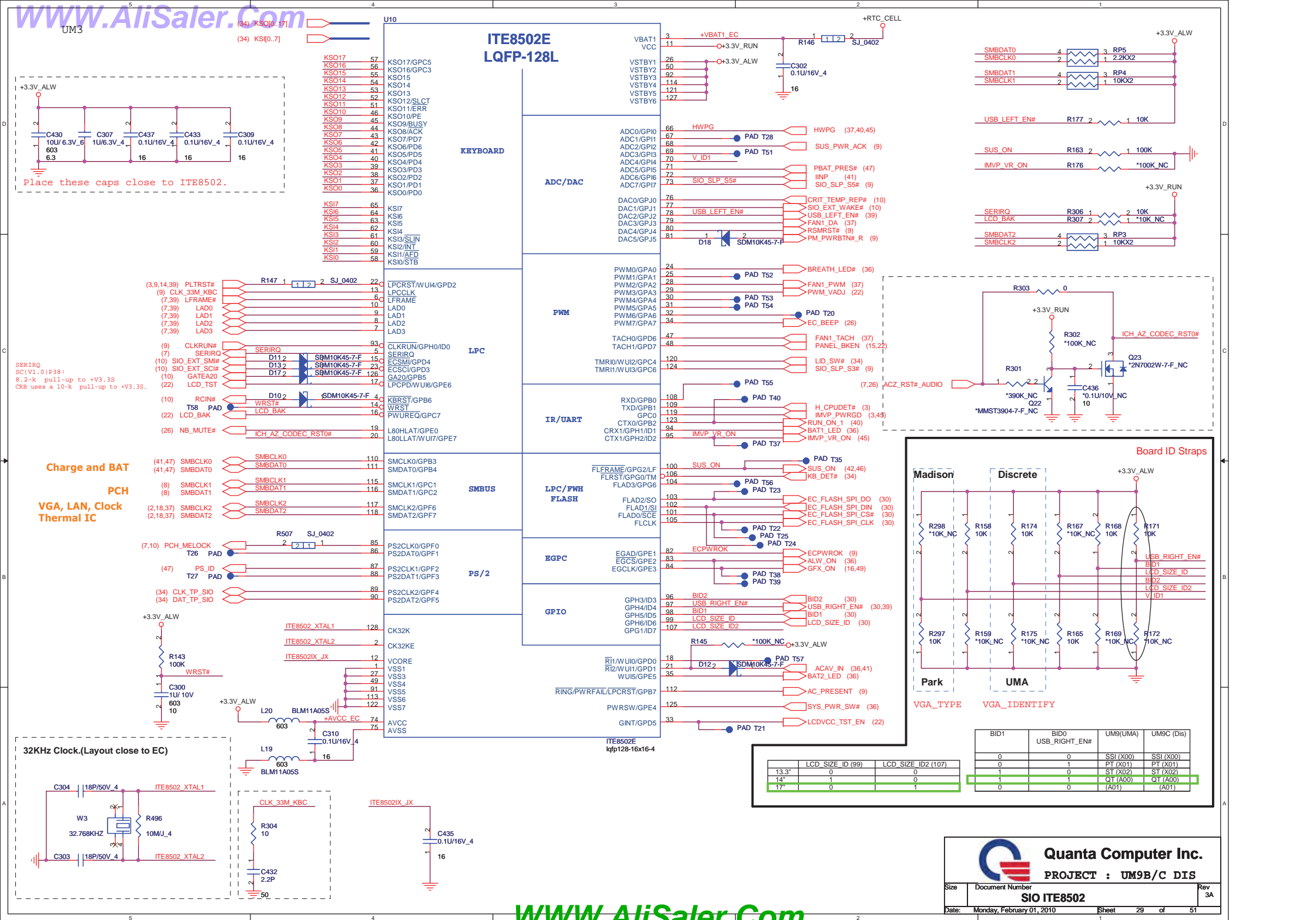




NB_MUTE#	TEST_WOOFER_EN	AUD_SPK PD#	SUB_MUTE#
0	0	L (Disable SPK)	L (Disable Woofer)
0	1	L (Disable SPK)	H (Test Woofer)
1	0	H (Test SPK)	L (Disable Woofer)
1	1	H (Test SPK)	H (Test Woofer)



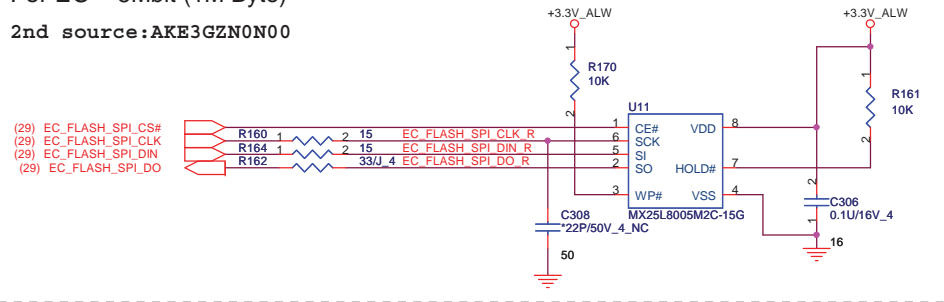




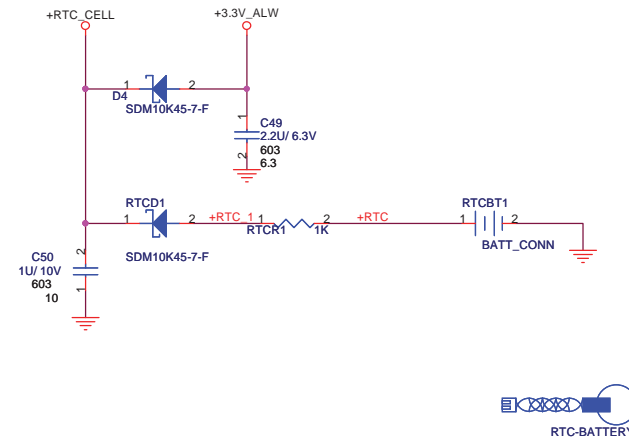
UM3

For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00



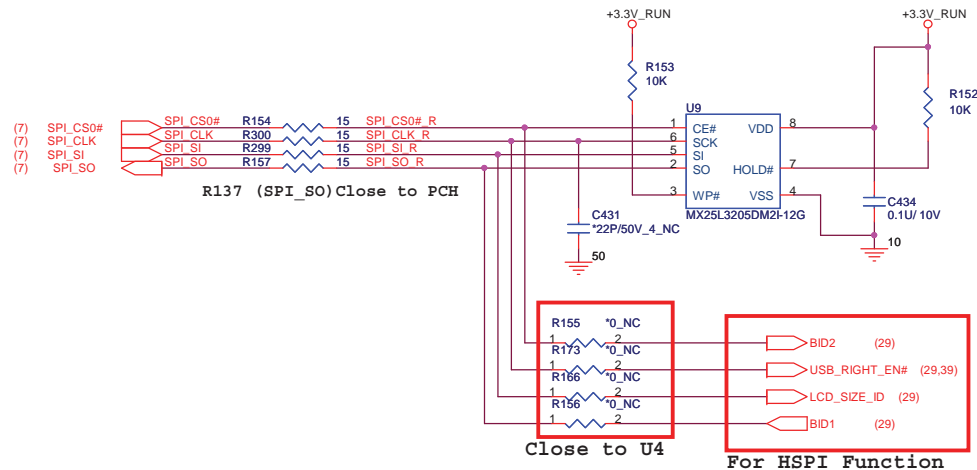
RTC BATTERY



For PCH

32Mbit (4M Byte)

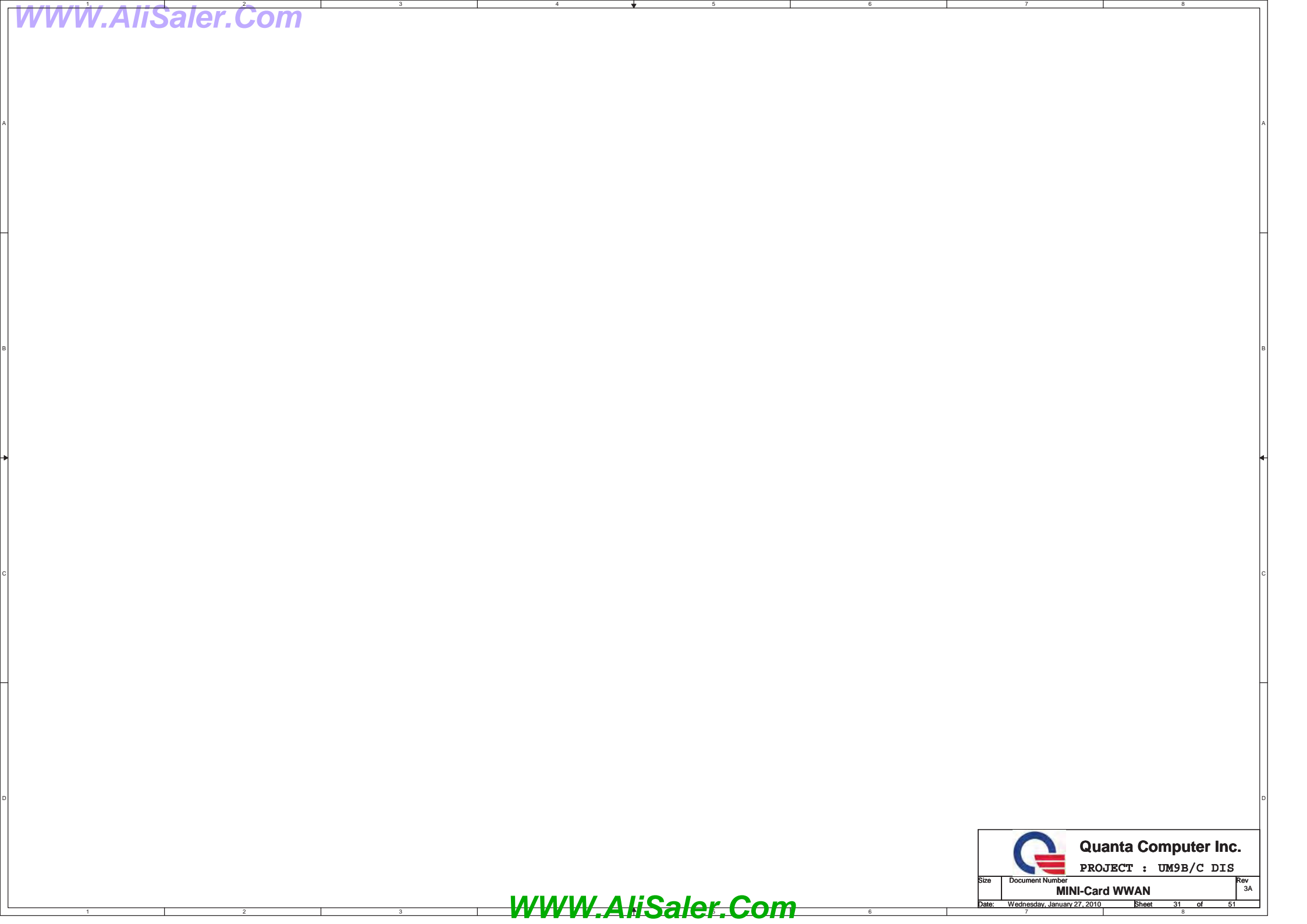
2nd source:AKE39ZP0N00



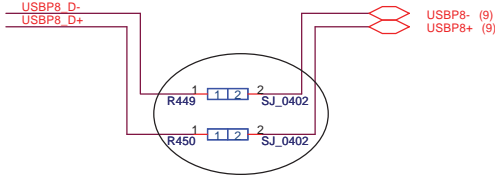
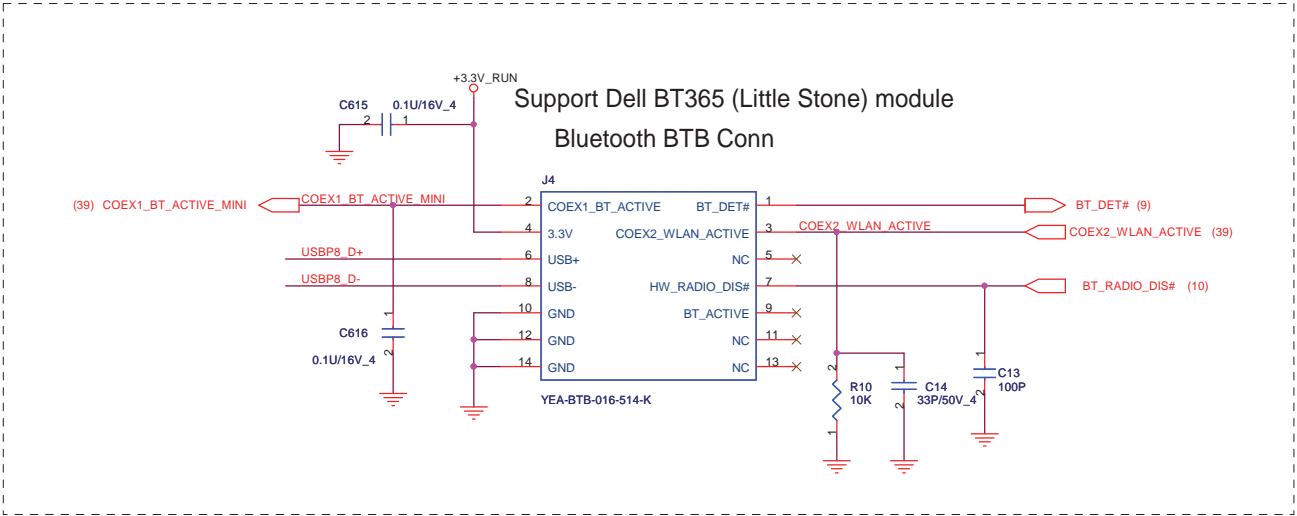
Quanta Computer Inc.

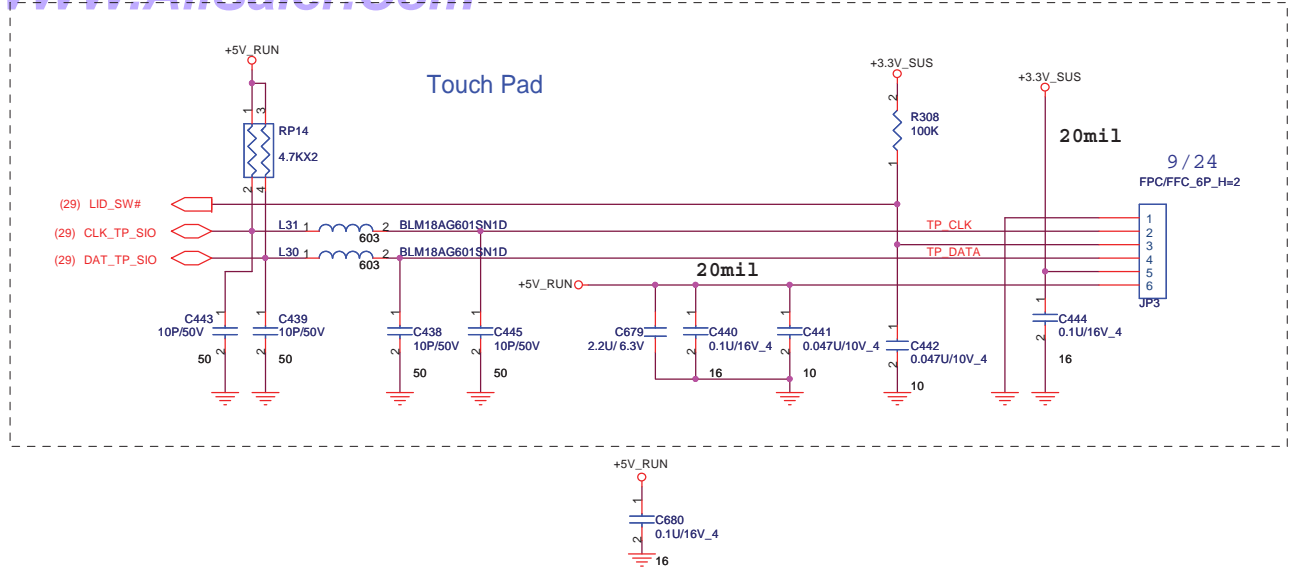
PROJECT : UM9B/C DIS

Size	Document Number	Rev
	FLASH/RTC	3A
Date:	Monday, February 01, 2010	Sheet 30 of 51

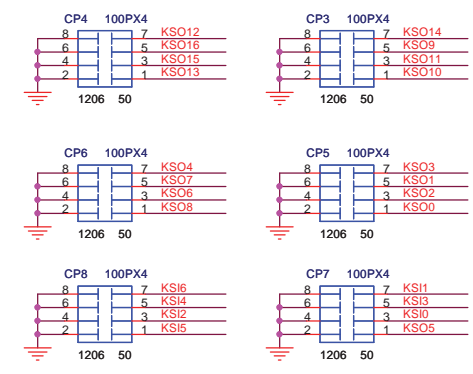
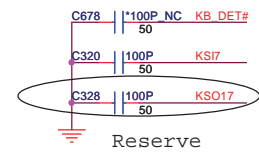
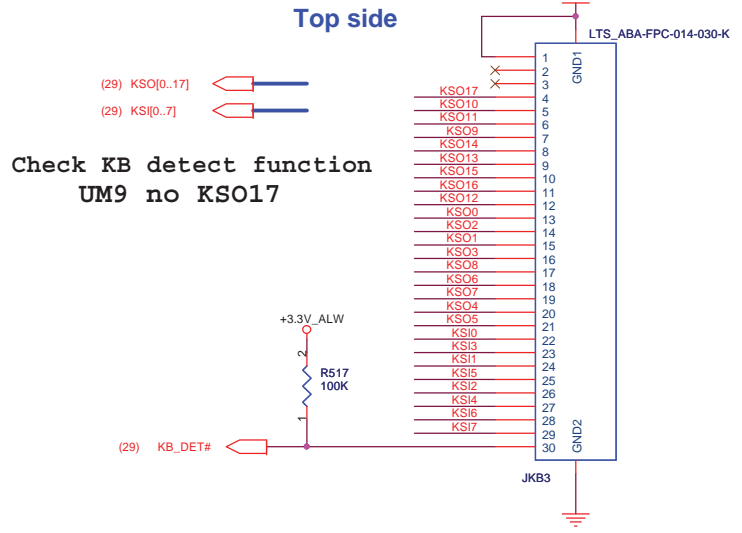


WLAN To DB





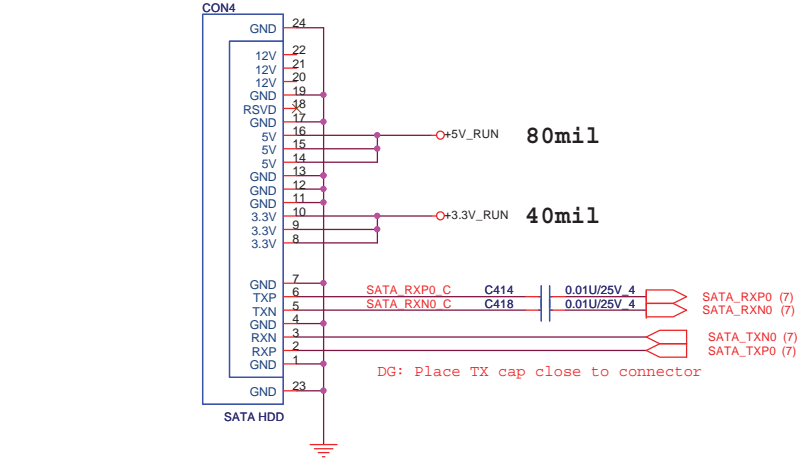
UM3 KEYBOARD CONNECTOR



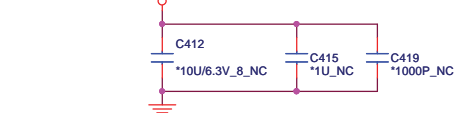
100P CAPS CLOSE TO JKB3

UM3

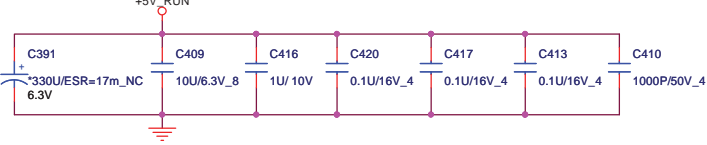
SATA Connector.



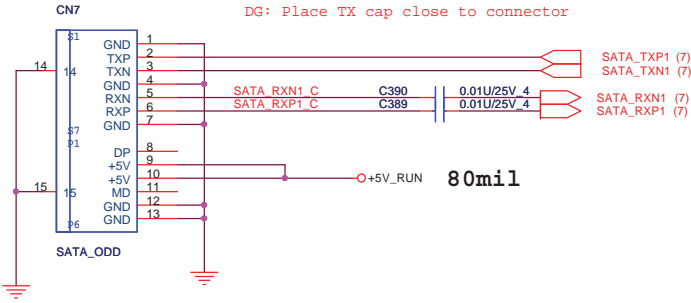
+3.3V_RUN Place caps close to connector.



Place caps close to connector.

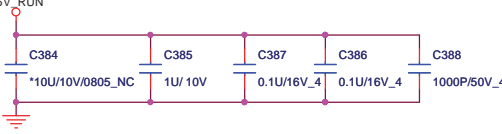


ODD Connector



DG: Place TX cap close to connector

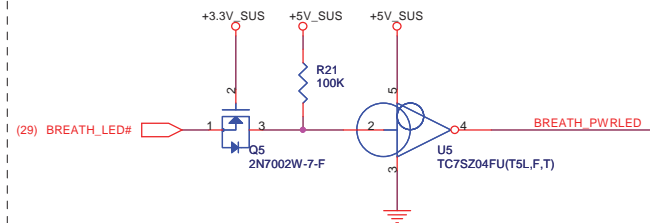
Place caps close to connector.



Quanta Computer Inc.
PROJECT : UM9B/C DIS

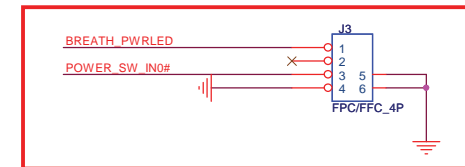
Size	Document Number	Rev
	SATA (HDD&CD_ROM)	3A
Date:	Monday, February 01, 2010	Sheet 35 of 51

Power

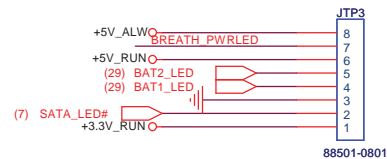


UM3

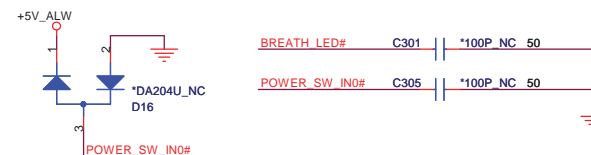
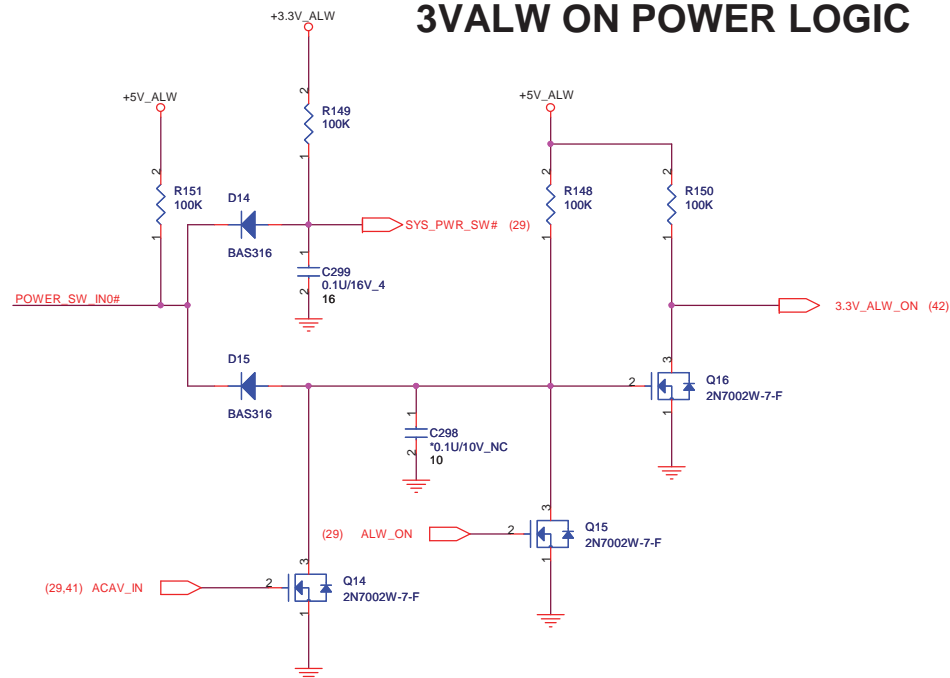
Power button Cable



Check Connector P/N and footprint



3VALW ON POWER LOGIC

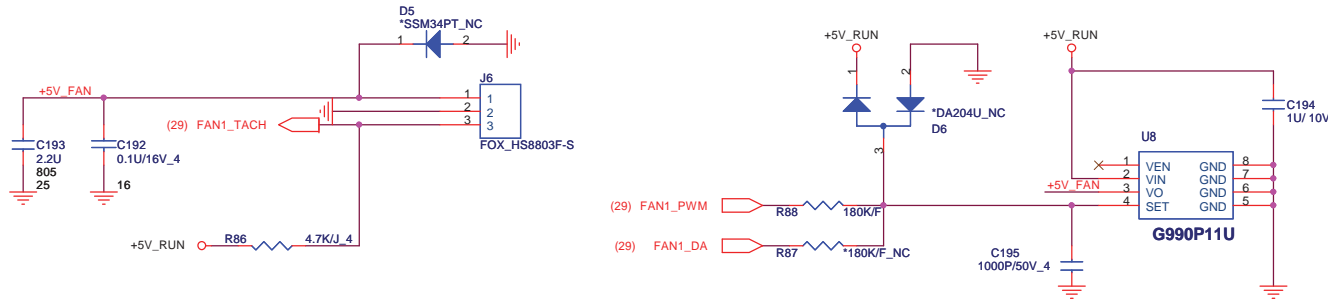


Quanta Computer Inc.
PROJECT : UM9B/C DIS

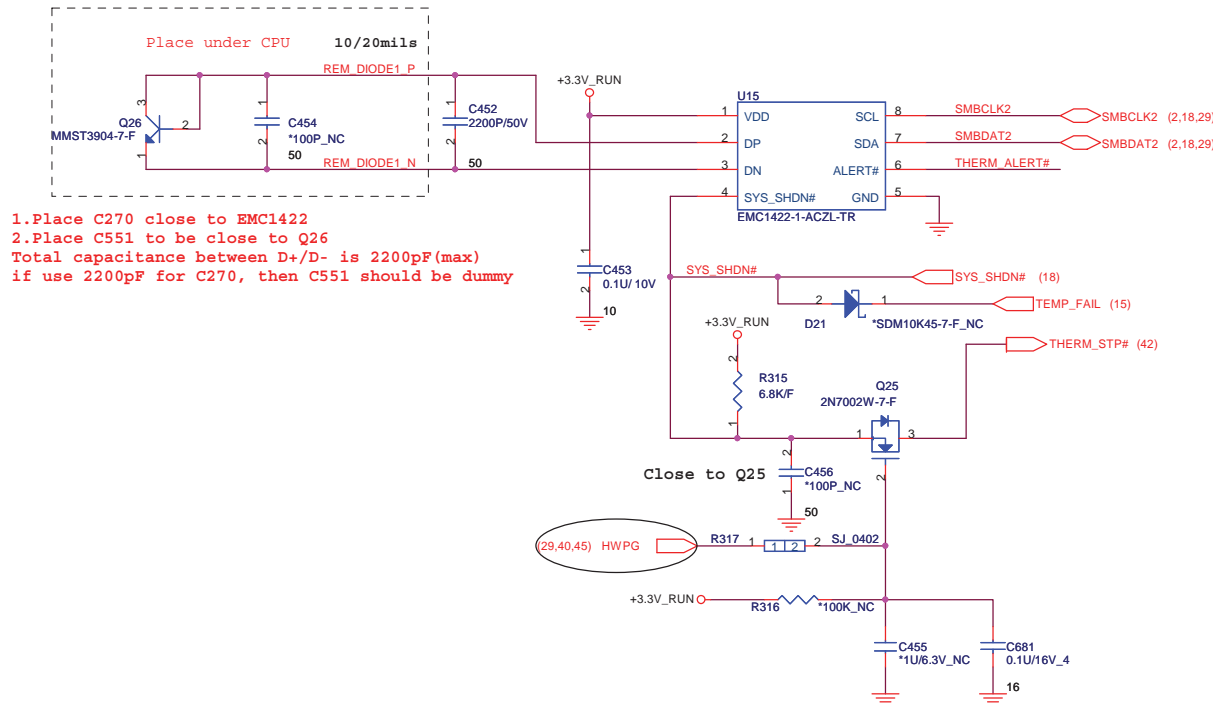
Size	Document Number	Rev
	SWITCH, LED	3A
Date:	Monday, February 01, 2010	Sheet 36 of 51

FAN CONTROL

6/23 COPY FROM RM6



UM3



- 1.Place C270 close to EMC1422
 - 2.Place C551 to be close to Q26
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C270, then C551 should be dummy


OTP 85 degree C



Quanta Computer Inc.

PROJECT : UM9B/C DIS

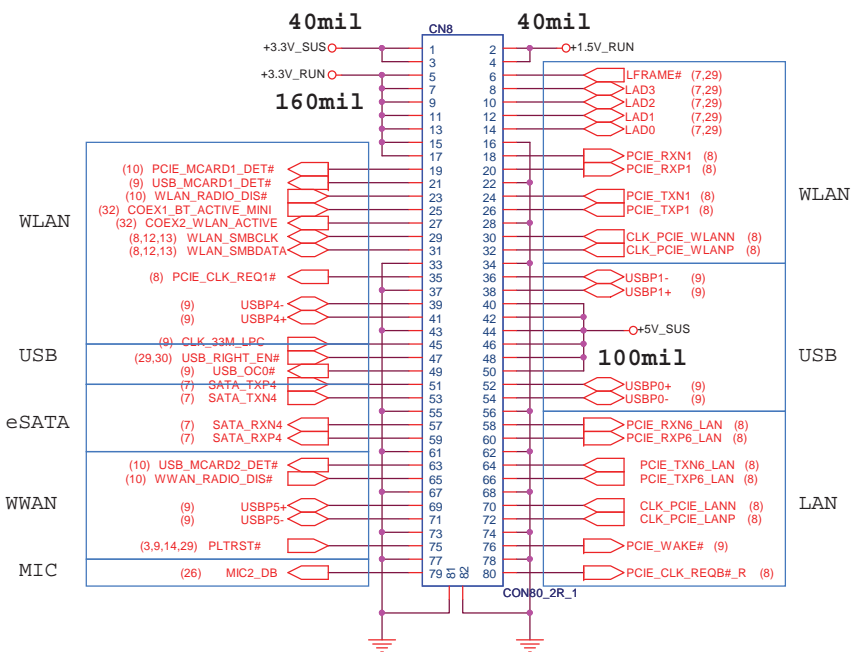
Size	Document Number	Rev
	FAN & THERMAL	3A
Date:	Monday, February 01, 2010	Sheet 37 of 51



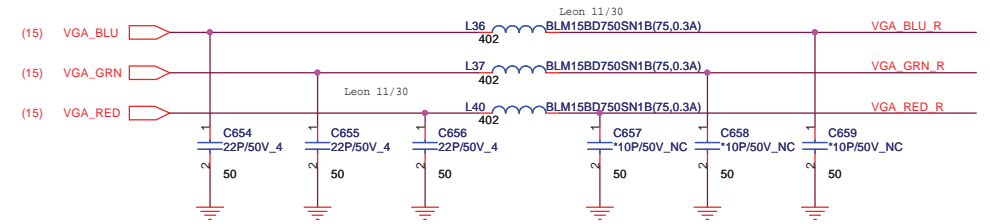
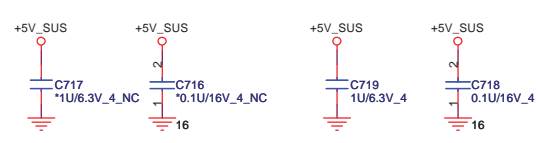
Quanta Computer Inc.

PROJECT : UM9B/C DIS

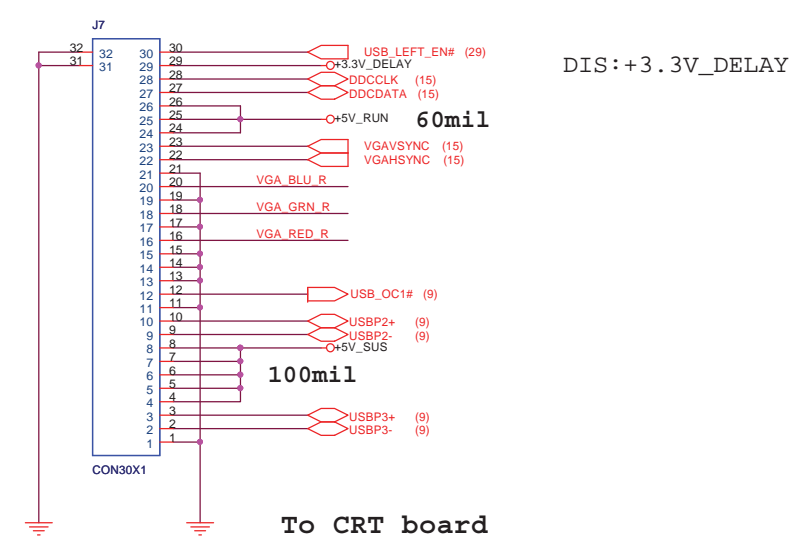
Size	Document Number	Rev
	LAN(AR8152/RJ-45)	3A
Date:	Wednesday, January 27, 2010	Sheet 38 of 51



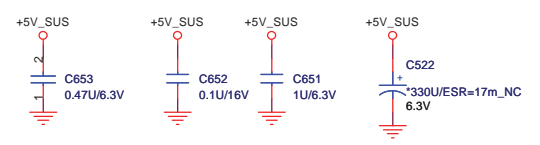
To DB

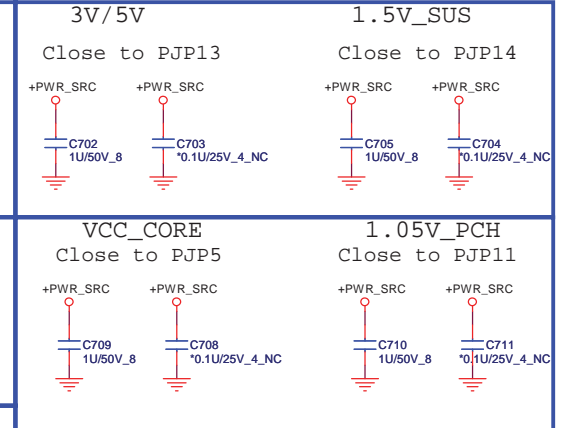
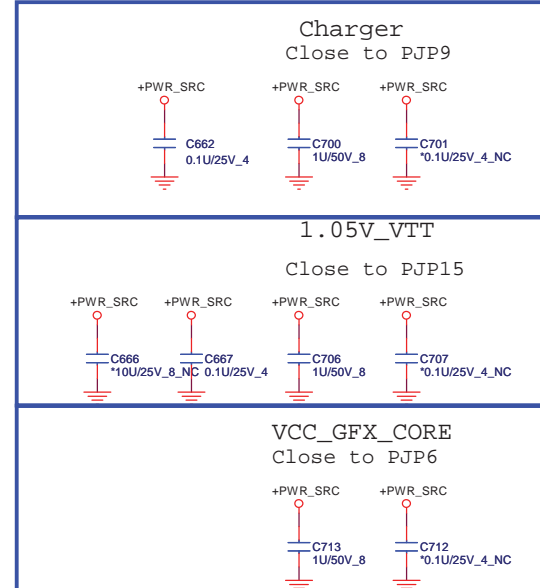
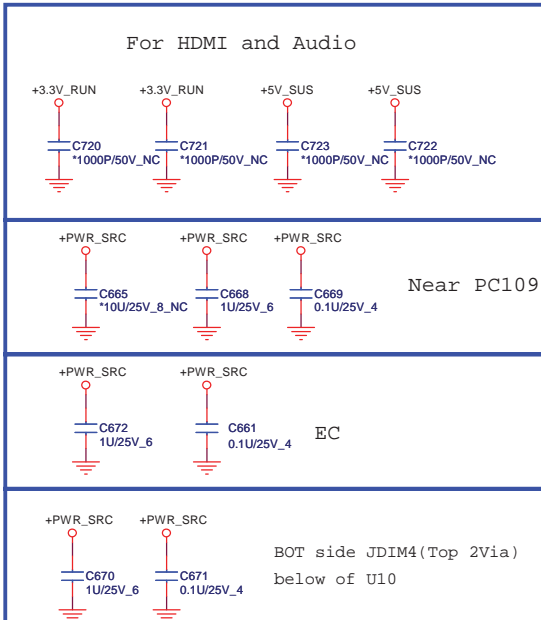
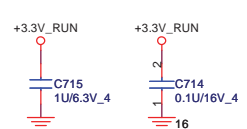
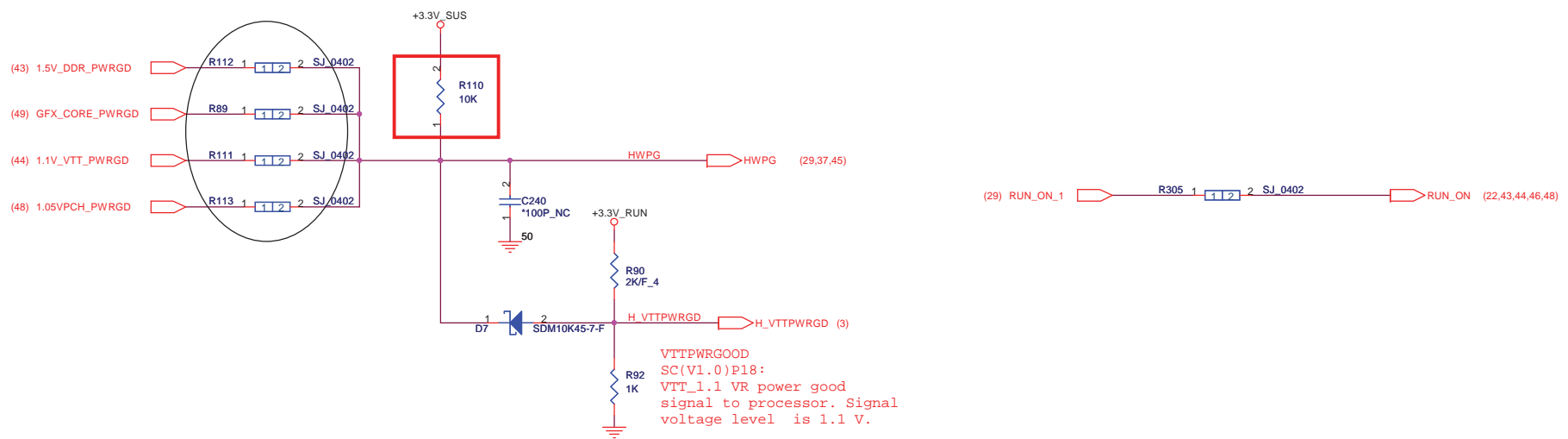


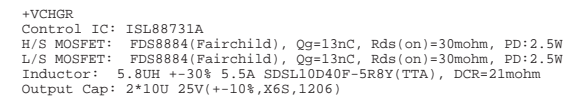
Close to VGA

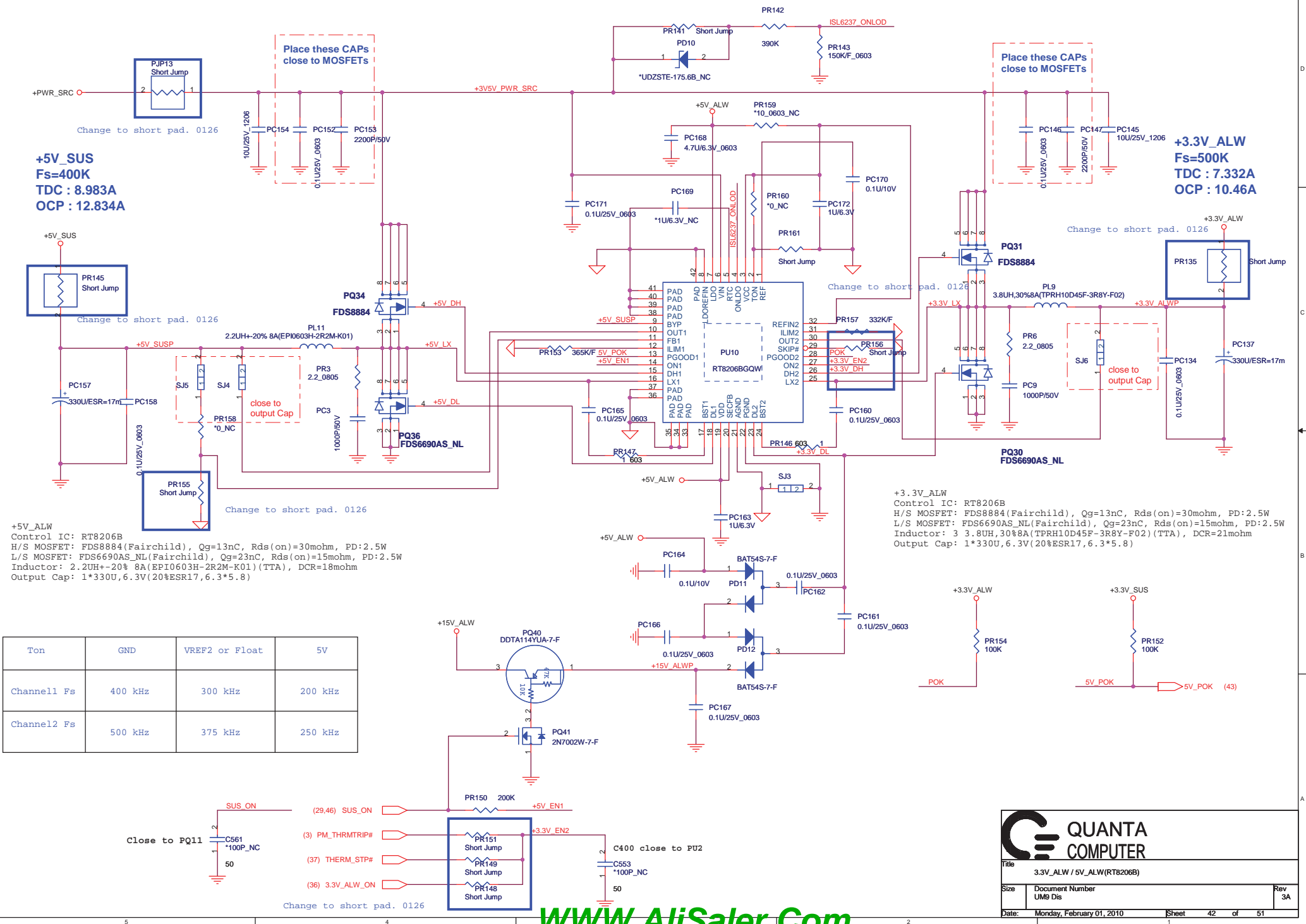


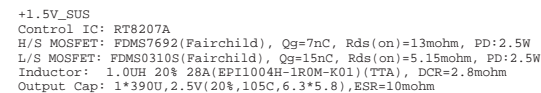
DIS:+3.3V_DELAY





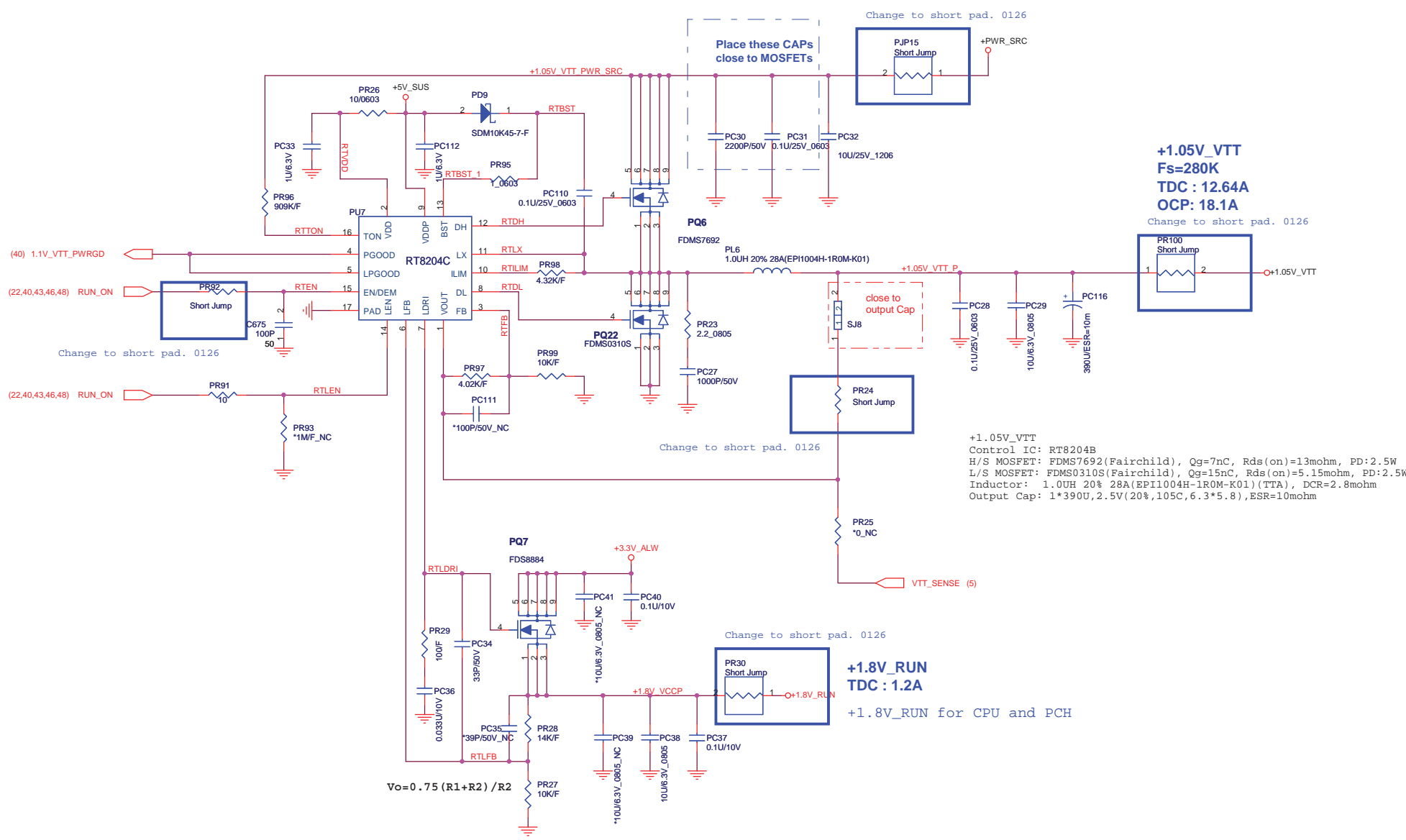




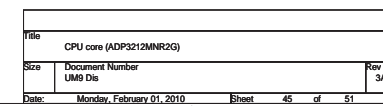


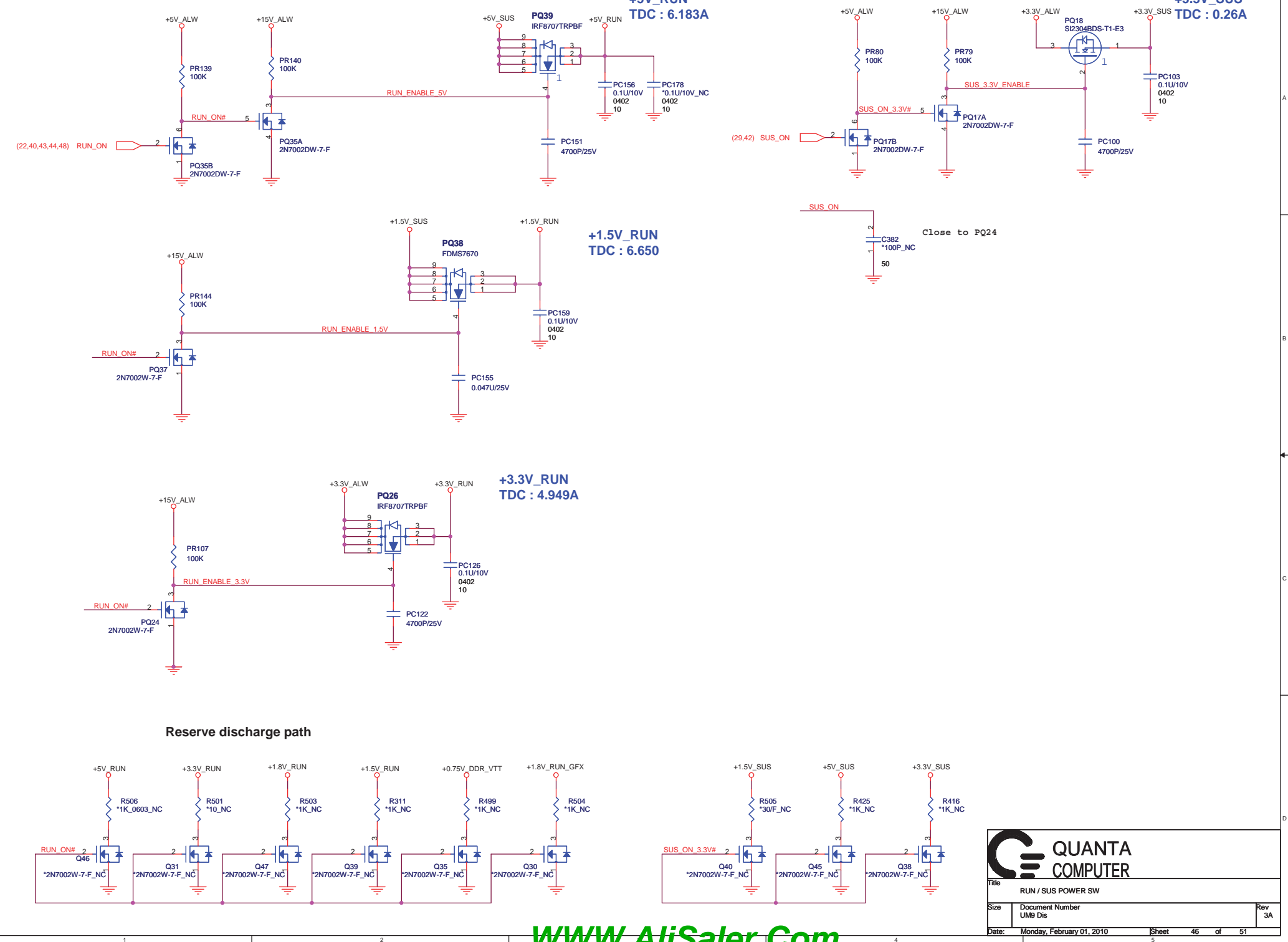
Outputs Management by S3, S5 control


State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)



Title				
+1.05V_VTT(RT8204C)				
Size	Document Number UM9 Dis			Rev 3A
Date:	Monday, February 01, 2010	Sheet	44	of 51

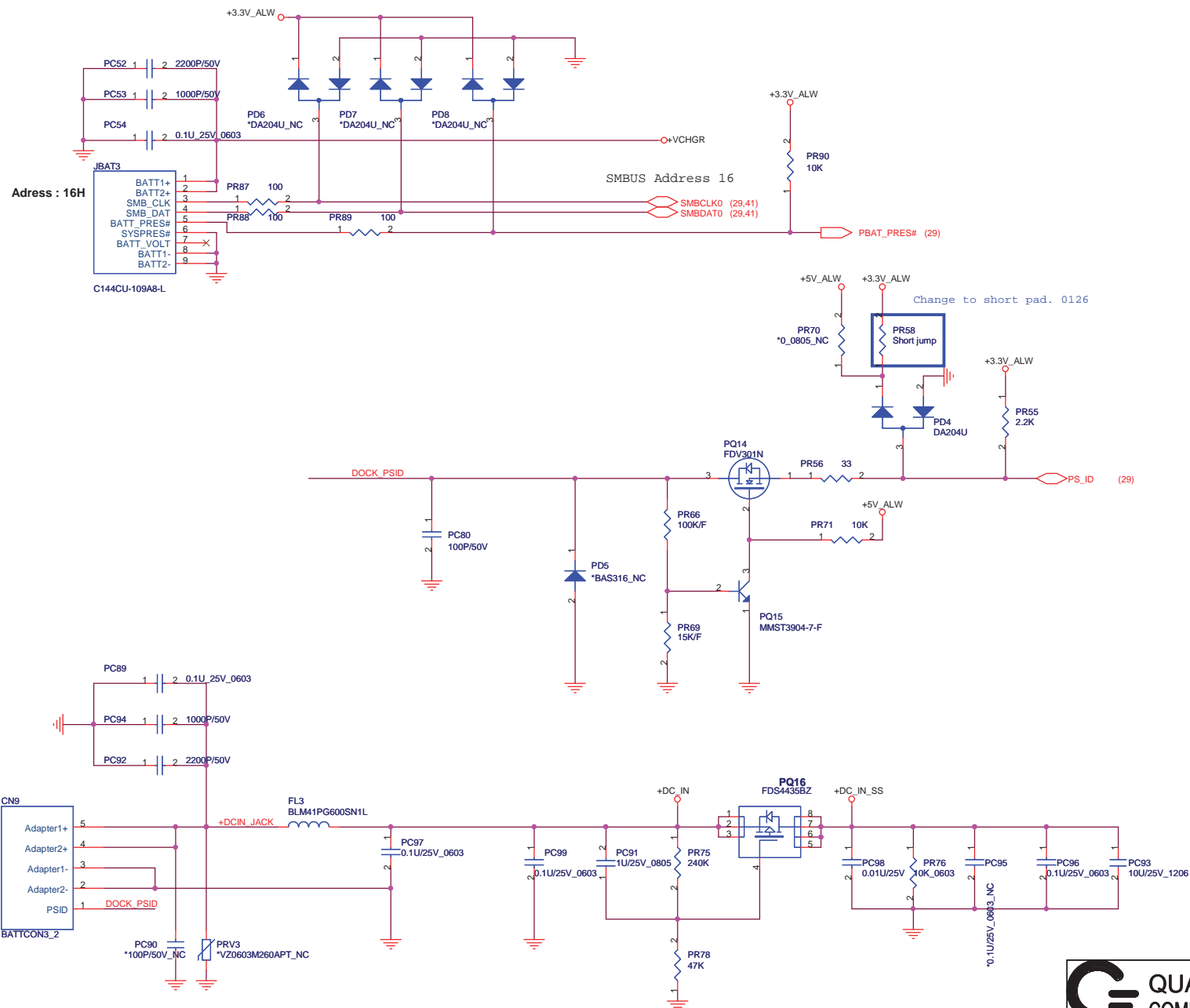






QUANTA
COMPUTER

Title RUN / SUS POWER SW		
Size	Document Number UM9 Dis	Rev 3A
Date:	Monday, February 01, 2010	Sheet 46 of 51



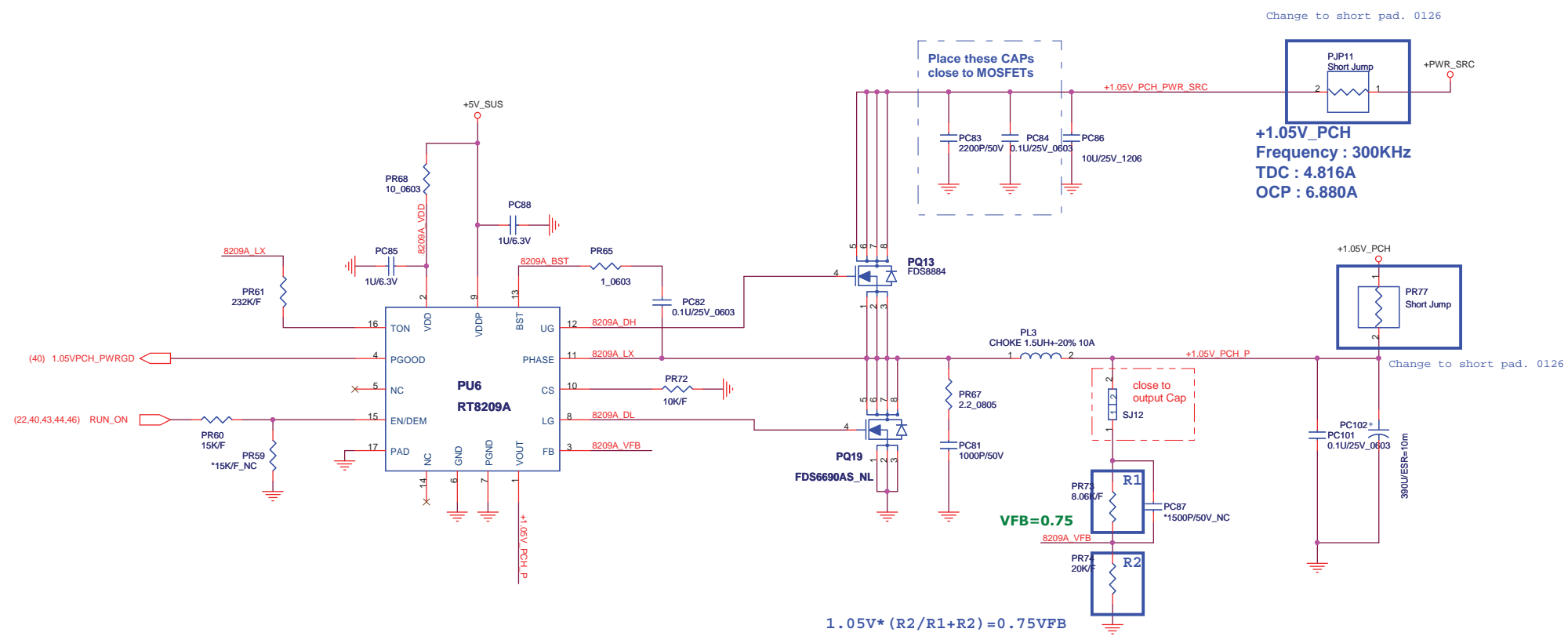
Title DCIN, BATT CONNECTOR

Size Document Number UM9 Dis

Rev 3A

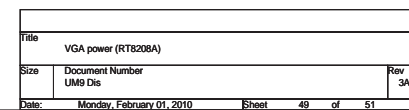
Date: Monday, February 01, 2010

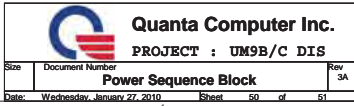
Sheet 47 of 51



+1.05V_PCH
Control IC: RT8209A
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
Inductor: 1.5uH+-20% 9A (10D40F-1R5M)(TTA), DCR=10.5mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm

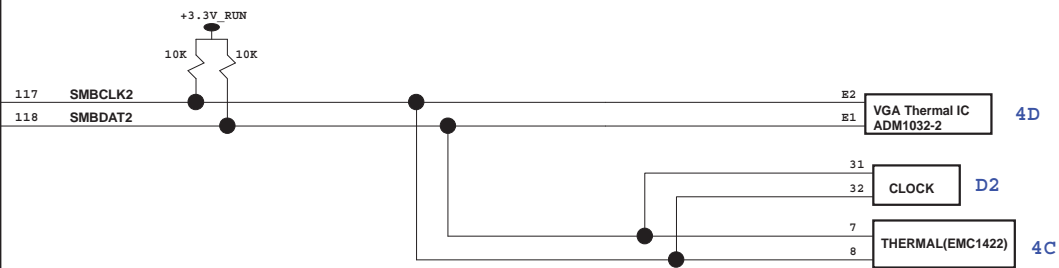
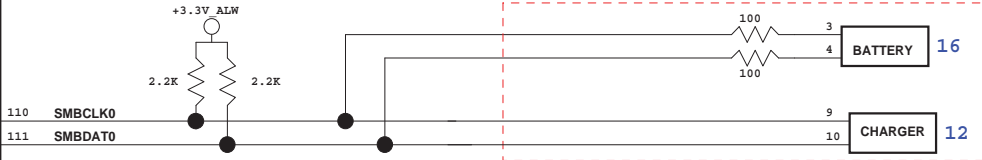
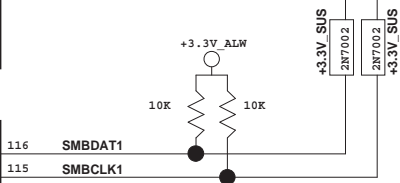
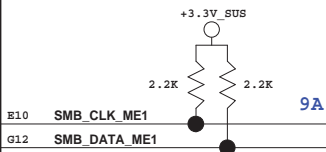
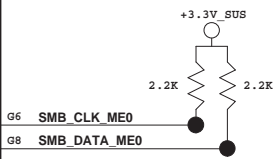
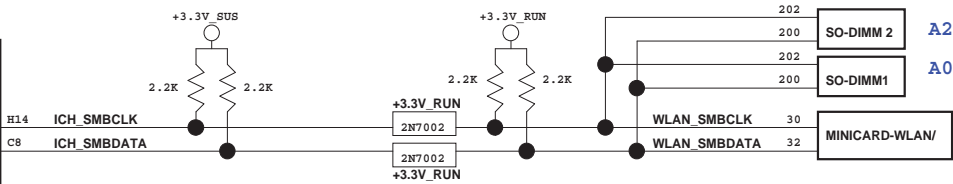
Title +1.05V_PCH(RT8209A)				
Size	Document Number UM9 Dis			Rev 3A
Date:	Monday, February 01, 2010	Sheet	48 of 51	





PCH

SIO
ITE8502



Function	IC	SMBus Address
Clock GEN	SLG8SP585VTR RTM875N-632	11010010 (D2h) D2h
DDR3	DIMM0 DIMM1	A0 A2
VGA	Madison, Park	0x41
Thermal IC	EMC1422	0100 1100b (4Ch)
VGA Thermal	ADM1032-2	4D
Charge IC	ISL88731A	0b0001001 (0x12)
	Battery	16h
	WLAN Module	X